Design Example Report

Title	***2-wire Forward / Reverse Phase BLE Smart Dimmer using LinkSwitch™-TNZ LNK3302D with Lossless AC Zero-Crossing Detection***
Specification	90 VAC – 305 VAC Input; 7 V / 70 mA Output
Application	Home and Building Automation, Lighting Control
Author	Applications Engineering Department
Document Number	DER-865
Date	July 23, 2021
Revision	1.1

Summary and Features

- Compatible with 2-wire (no neutral) and 3-wire home/building wiring
- Highly integrated non-isolated power supply with LNK3302D
- Low-component count with integrated 725 V power MOSFET, current sensing and protection
- Lossless Zero-crossing signal output synchronized to AC line
- Wide-range AC input
- User selectable forward (leading-edge) or reverse (trailing-edge) dimming mode
- Compatible with 3 W to 250 W low-PF and high-PF dimmable lamps
- <200 µA standby input current (including BLE) across AC line
- Meets EN55022 and CISPR-22 Class B conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a two-wire (optional Neutral) Bluetooth Low Energy (BLE) smart wall dimmer using LinkSwitch-TNZ LNK3302D. Dimming is configurable as either Forward-phase (Leading-edge) or Reverse-phase (trailing-edge) mode using back-to-back MOSFETs.

The power supply is configured as a high-side buck converter designed to provide a nominal output voltage of 7 V at 70 mA load from a wide input voltage range of 90 VAC to 305 VAC. The lossless zero-crossing detection (ZCD) circuit provides the line information to the Nordic NRF52832 BLE module.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

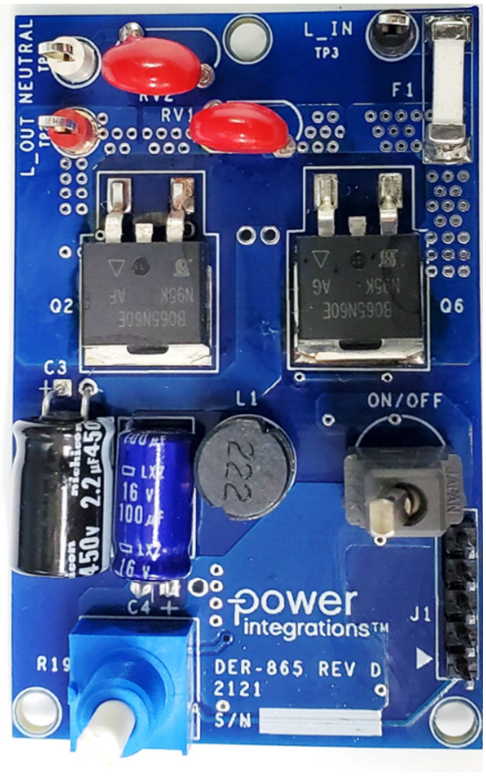

Figure 1 – Populated Circuit Board, Top View.

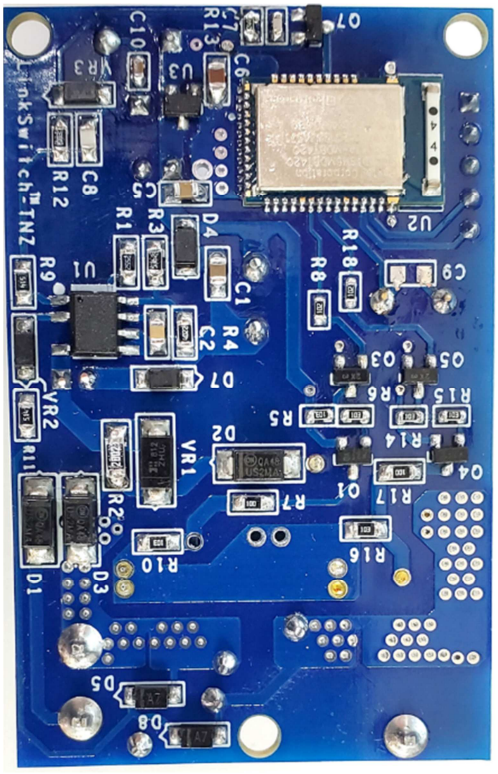

Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		305	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
No-load Input Current			200		µA	
Output						
Output Voltage	V_{OUT}		7		V	± 5%.
Output Current	I_{OUT}		0.07		A	
Total Output Power						
Continuous Output Power	P_{OUT}		0.49		W	
Efficiency						
Full Load	η		69		%	Measured at P_{OUT} 25 °C.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC 60950-1				
Surge			1		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Surge: 2 Ω.
Ring Wave			2.5		kV	Ring Wave: 12 Ω.

3 Schematic

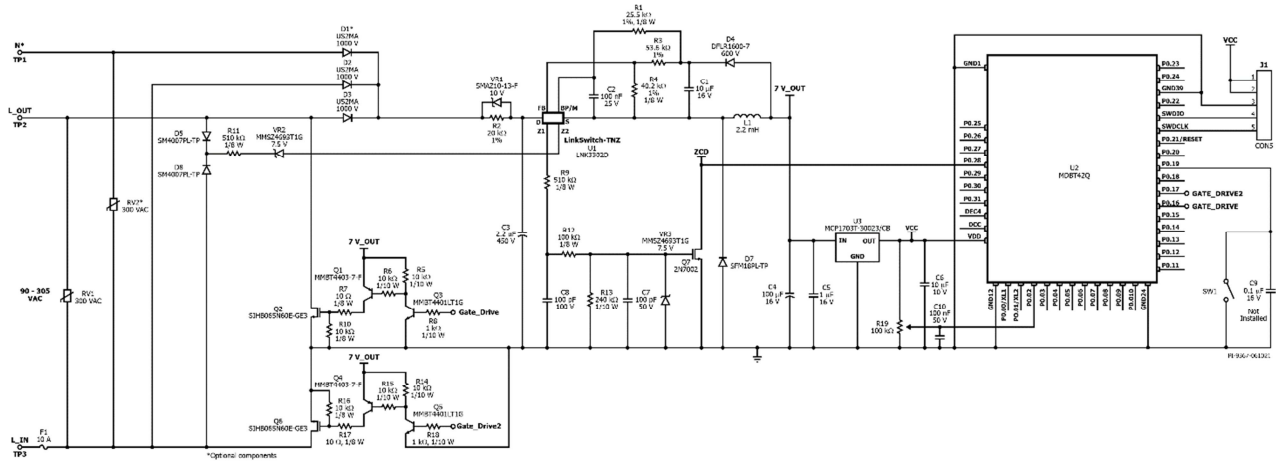

Figure 3 – Schematic.

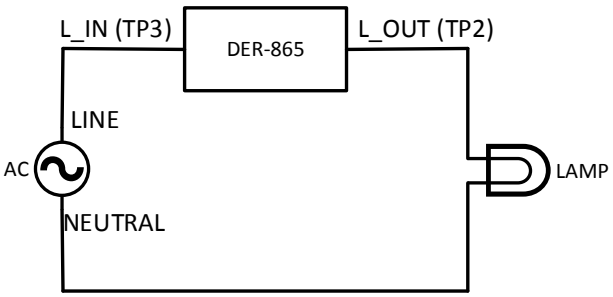

Figure 4 – 2-Wire Connection Diagram.

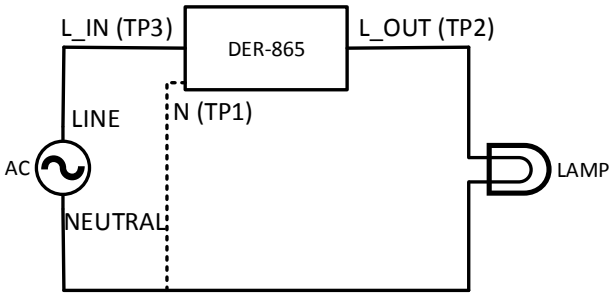

Figure 5 – 3-Wire Connection Diagram.

4 Circuit Description

4.1 *LinkSwitch-TNZ Block*

4.1.1 Input Stage

In two-wire configuration (figure 4), the AC input voltage is full-wave rectified by diodes D2 and D3. In 3-wire mode (figure 5), D1 is also used for rectification. The rectified DC is filtered by the bulk storage capacitor C3.

4.1.2 Input Protection

Fuse F1 provides safety protection against catastrophic circuit failures. Varistors RV1 and RV2 protect against surge events.

4.1.3 Power Factor Circuit

The proprietary R-Z circuit R2 and Zener diode VR1 minimizes the no-load input current that is important in many 2-wire switch or dimmer applications. VR1 is rated 1W with a 10V clamping voltage. Higher Zener voltage may reduce no-load input current further, but it might cause higher power dissipation during surge. Resistor R1 is tuned either at no-load or at standby, whichever is applicable. The resistance is set such as its peak voltage is just below the Zener voltage. This yields the lowest input current.

4.1.4 LNK3302D Power Supply Operation

LinkSwitch-TNZ combines a high-voltage power MOSFET switch, a power supply controller, and a Zero Crossing Detector in a single device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-TNZ uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TNZ controller consists of an oscillator, feedback (sense and logic) circuit, 5 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a 725 V power MOSFET.

This design is configured as a high-side buck converter using U1 LNK3302D. At AC start-up, the device starts switching once the BYPASS (BP/M) pin voltage charges to V_{BP}. A 100 nF capacitor C2 connected to BP sets the current limit to standard. Resistor R1 provides external bias to the BP/M pin and reduces the no-load input power by setting R1 to provide about 75 μA (I_{S1}) to the BYPASS pin.

When the MOSFET turns ON, current flows to the load via inductor L1. Energy is stored in the inductor, and the output capacitor C4 gets charged. When the MOSFET turns OFF, the stored energy from L1 is released to the load via free-wheeling diode D7. The charge stored in C4 supplies the current until the next switching event occurs. Diode D7 must be an ultrafast diode with a reverse recovery time (trr) of 35 ns or less. This is because the converter operates in Continuous Conduction Mode (CCM).

4.1.5 Feedback and Output Voltage Regulation

In this high-side buck, direct feedback configuration, the rectified voltage across L1 via D4 and C1 tracks the output voltage. Resistors R3 and R4 divides the voltage such that the FB pin is set to 2 V. When the current delivered into this pin exceeds I_{FB} (49 µA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds $I_{FB,}$ then subsequent cycles will be skipped until the current reduces below I_{FB}. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped.

4.1.6 Zero-Crossing Detection

Z1 and Z2 pins provide a lossless (<5 mW) zero-crossing detection (ZCD) signal. The input sensing circuit is comprised of rectifier diodes D5 and D8, series resistor R11 and a 7.5 V Zener diode VR2 connected to Z2 pin. The output signal from Z1 drives transistor Q7 through series resistor R9, filter components C8, R12, and C7, gate pull-down resistor R13, and gate Zener diode VR3. The drain of Q7 is the ZCD output that is connected to pin 5 (P0.28) of U2.

The value of VR2 is selected to be 7.5 V to allow sufficient time for the gate of Q7 to turn OFF at zero crossing. Series resistors R9 and R11 reduce conducted EMI by suppressing switching noise coupled to Z1/Z2 pins from being transmitted to the AC input. The filter network C8, R12, and C7 are needed to ensure ZCD signal integrity while minimizing the delay. VR3 protects the gate of Q7 and R13 is needed to ensure that the gate capacitance is discharged properly. Lower value could lead to premature detection of the ZCD since the current from Z1/Z2 pins is limited to 22 µA. Consequently, a high value of R13 may cause the ZCD signal to work improperly, especially when connecting a voltage probe.

It is important to use a differential voltage probe when probing the ZCD.

At start-up, both power MOSFETS Q2 and Q6 are OFF initially. The ZCD output (Q7 drain) is normally low due to signal rectification via D5 and D8. As the input voltage approaches zero crossing, the Zener diode VR2 becomes reversed-biased and blocks current from flowing to Q7 gate. The MOSFET briefly turns OFF and this short pulse provides zero crossing signal to the microcontroller. While dimming is still possible without sensing the ZCD in standby mode, doing so allows a soft-start when the dimmer turns ON and reduces start-up inrush current.

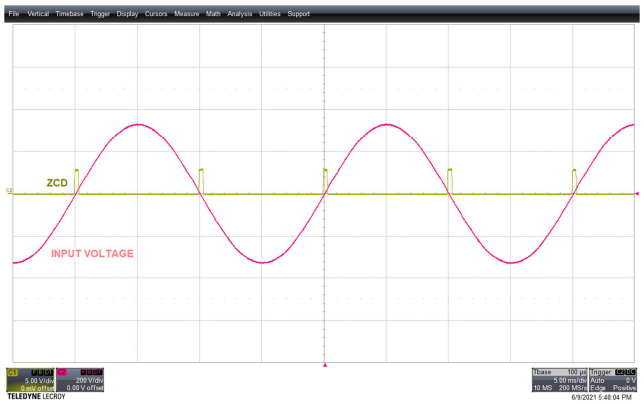

Figure 6 – ZCD Signals in Standby Mode (Light Off).

In leading-edge dimming mode, the ZCD sensing is done every high-to-low transition. The delay (<500 μs) is due to the filter network and may be compensated through software adjustments. Fine-tuning the value of R13 may also reduce the delay. In trailing-edge dimming mode, the ZCD sensing is done every low-to-high transition.

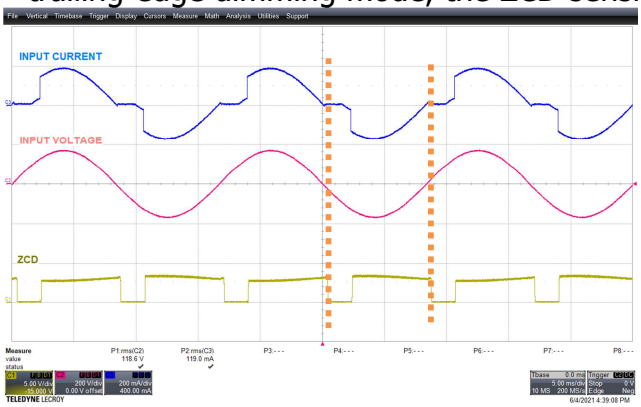

Figure 7 – Leading-Edge Mode ZCD Detection.

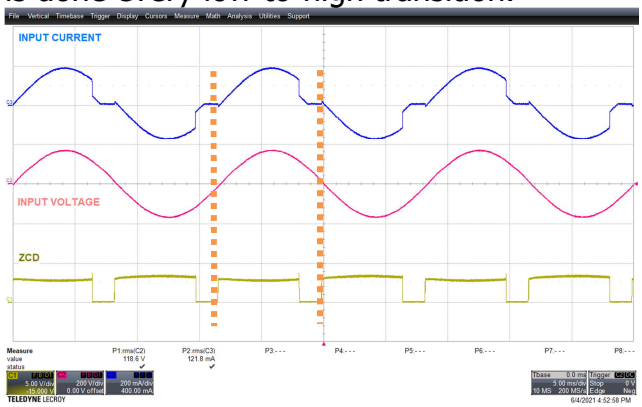

Figure 8 – Trailing-Edge Mode ZCD Detection.

4.2 *Back-to-Back MOSFETs*

This DER uses two 650 V, 57 mΩ MOSFETs (Q2, Q6) in back-to-back configuration as the main phase-cut dimming elements. They can work in forward-phase or reverse-phase dimming mode.

The outputs from the BLE module U2, Gate_Drive and Gate_Drive2, drive Q3 and Q5 bases via limiting resistors R8 and R18. Resistor R5 and R14 are collector bias resistors for Q3 and Q5. When these transistors turn ON, the PNP transistors Q1 and Q4 will also turn ON and drive the gate of the power MOSFETs Q2 and Q6. Resistors R6, R7, R15, and R17 are current-limiting resistors. When the gate drive signals go low, Q2 and Q6 will turn OFF. Resistors R10 and R16 are gate pull-down resistors. The power MOSFETs are only switching every half-line cycle. Hence, the switching losses due to slower turn-off time is negligible compared to conduction losses. A low $R_{DS(ON)}$ MOSFETs are required for Q2 and Q6 to be able handle higher power. For simplicity, these MOSFETs use the PCB as the heatsink. However, in applications that require higher power, heatsinks are normally used.

When selecting the power MOSFETs, please note that they also have leakage current in OFF state and may contribute to higher standby current. For single-line application (low-line or high-line only), it is easier to find a MOSFET that is optimized for lower leakage current. This DER showcases a wide-range input capability that requires high-voltage MOSFETs with very low $R_{DS(ON)}$. The leakage current from the MOSFETs adds about 70 μA to the overall unit consumption. Despite this, this DER achieves <200 μA standby current.

4.3 *3V Linear Regulator*

A low-dropout regulator U3 provides a stable 3 V supply to the BLE module. Capacitors C5 and C6 are used to stabilize the regulator.

4.4 *BLE Module*

This DER uses a Bluetooth5-certified Bluetooth Low-Energy (BLE) module, MDBT42Q, based on Nordic NRF52832 SoC. Its ultra-low current consumption, together with LinkSwitch-TNZ power supply and lossless ZCD, enables a <200 μA standby input current (with BLE connected).

4.4.1 Pin Functions

Pin Number	Description
15 (P0.02)	Configured as ADC Input. The pin detects the voltage across the 100 k potentiometer R19. The potentiometer serves as dimming control. Capacitor C10 provides filtering for the ADC input.
30 (P0.16)	Configured as Digital Output. It provides the gate drive pulse to MOSFET Q2.
31 (P0.17)	Configured as Digital Output. It provides the gate drive pulse to MOSFET Q4.
33 (P0.19)	Configured as Digital Input. Senses the push-button switch SW1 to trigger dimmer ON/OFF. C9 (not installed) provides passive de-bouncing to ensure clean input signal when the switch SW1 is pressed.
36 (SWDCLK)	Programming pin.
37 (SWDIO)	Programming pin.
11 (VDD)	The VDD comes from the 3V LDO regulator.
1, 12, 24, 39	Ground.

4.4.2 App-based Dimming

To download the app, search for DER-865 in the Apple App Store.

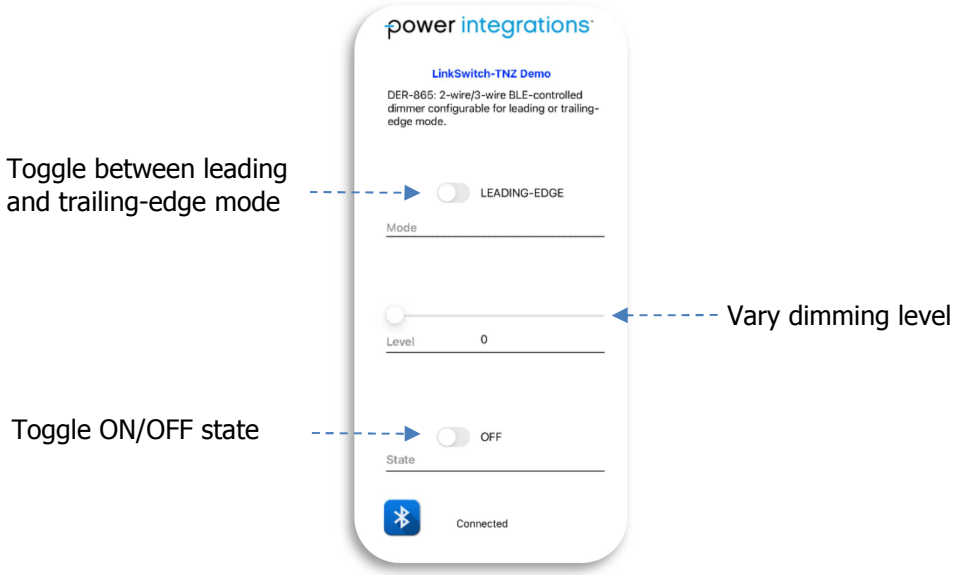

Figure 9 – Mobile app interface.

When the leading-edge/trailing-edge mode button is pressed, the dimmer will turn-off. Set the ON/OFF switch to ON-state (using the app or using the physical switch SW1) to enable the dimmer.

4.4.3 Manual Dimming

Toggle the ON/OFF switch (SW1) to turn-on or turn-off the dimmer. Rotate the potentiometer R19 knob to change the dimming level. Manual dimming via R19 will stop responding once dimming via app is activated. To re-enable manual dimming, toggle SW1 from OFF to ON.

5 PCB Layout

Board info: 2 layers, 2 oz. copper, FR4, 1.59 mm (0.062 in) thickness

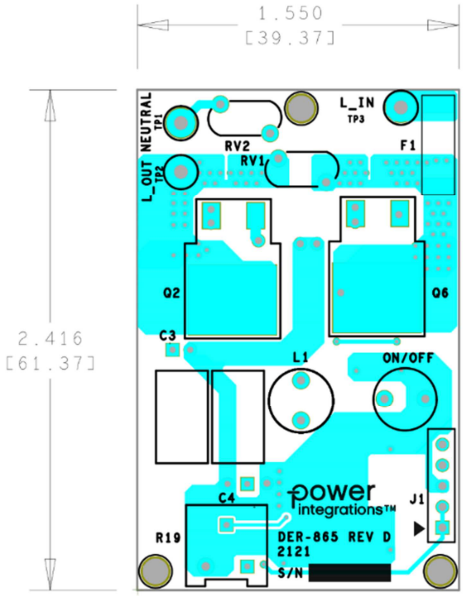

Figure 10 – Populated Circuit Board, Top View.

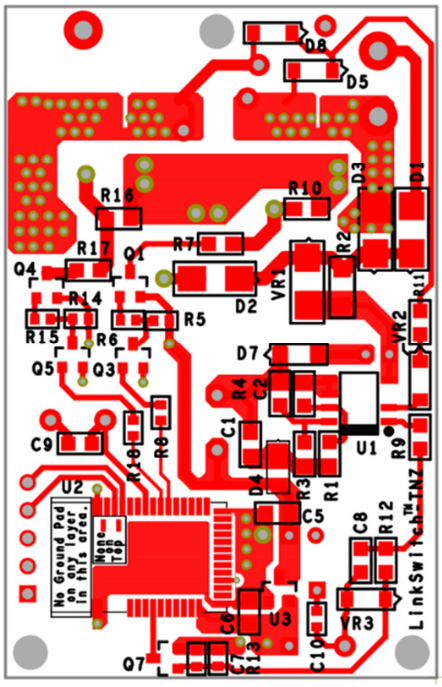

Figure 11 – Populated Circuit Board, Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C1	10 µF, ±10%, 16V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
2	1	C2	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
3	1	C3	2.2 µF, 450 V, Electrolytic, (8 x 11.5)	UVK2W2R2MPD1TD	Nichicon
4	1	C4	100 µF, 16 V, Electrolytic, Low ESR, 250 mΩ, (6.3 x 11.5)	ELXZ160ELL101MFB5D	Nippon Chemi-Con
5	1	C5	CER, 1 uF, 16V, X7R, 0805	GRM21BR71C105KA01K	Murata
6	1	C6	10 µF, 10 V, Ceramic, X7R, 0805	C2012X7R1A106M	TDK
7	1	C7	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
8	1	C8	100 pF 100 V 10 % X7R 0805	08051C101JAT2A	AVX
9	1	C9	0.1 µF, ±5%, 16V, X7R, 0805	C0805C104J4RACTU	Kemet
10	1	C10	100 nF, ±10%, 50 V, Ceramic, X7R, 0603	GCM188R71H104KA57J	Murata
11	1	D1	Diode, Standard, 1 kV, 1.5 A, SMT, SMA (DO-214AC)	US2MA	ON Semi
12	1	D2	Diode, Standard, 1 kV, 1.5 A, SMT, SMA (DO-214AC)	US2MA	ON Semi
13	1	D3	Diode, Standard, 1 kV, 1.5 A, SMT, SMA (DO-214AC)	US2MA	ON Semi
14	1	D4	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes Inc
15	1	D5	1000V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
16	1	D7	Diode, GEN PURP, 600 V, 1 A, SOD123FL, SOD-123F	SFM18PL-TP	Micro Commercial
17	1	D8	1000V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
18	1	F1	FUSE, BOARD MNT, 10 A, 250 VAC, 125VDC, Surface Mount, 2-SMD, Square End Block	3403.0176.11	Schurter
19	1	L1	2.2 mH, 0.18 A, Radial, 10%	RL875-222K-RC	Bourn
20	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
21	1	Q2	N-Channel, 600 V, 40 A (Tc), 250 W (Tc), SMT, D2PAK, D²PAK (TO-263)	SIHB065N60E-GE3	Vishay
22	1	Q3	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300 mW, SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semi
23	1	Q4	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
24	1	Q5	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300 mW, SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semi
25	1	Q6	N-Channel, 600 V, 40 A (Tc), 250 W (Tc), SMT, D2PAK, D²PAK (TO-263)	SIHB065N60E-GE3	Vishay
26	1	Q7	60 V, 115 mA, SOT23-3	2N7002-7-F	Diodes Inc
27	1	R1	RES, 25.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2552V	Panasonic
28	1	R2	RES, 20.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2002V	Panasonic
29	1	R3	RES, 53.6 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5362V	Panasonic
30	1	R4	RES, 40.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4022V	Panasonic
31	1	R5	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
32	1	R6	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
33	1	R7	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
34	1	R8	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
35	1	R9	RES, 510 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ514V	Panasonic
36	1	R10	RES, 10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
37	1	R11	RES, 510 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ514V	Panasonic
38	1	R12	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
39	1	R13	RES, 240 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ244V	Panasonic
40	1	R14	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
41	1	R15	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
42	1	R16	RES, 10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
43	1	R17	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
44	1	R18	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
45	1	R19	POT, 100 kΩ, 20%, 1/2 W, Square Trimming	3310Y-001-104L	BOURNS
46	1	RV1	300 VAC, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
47	1	RV2	300 VAC, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse

48	1	U1	LinkSwitch-TNZ, SO8	LNK3302D	Power Integrations
49	1	U2	MDBT42Q, (Nordic nRF52832 BASED BLE MODULE)	317030213	Seeed Technology
50	1	U3	IC, REG, LINEAR, 3V, 250MA, SOT-23-3	MCP1703T-3002E/CB	Microchip
51	1	VR1	Diode, Zener, 10 V, ±5%, 1 W, DO-214AC, SMA	SMAZ10-13-F	Diodes Inc
52	1	VR2	Diode, Zener, 7.5V, ±5%, 500 mW, SOD123, 150°C	MMSZ4693T1G	ON Semi
53	1	VR3	Diode, Zener, 7.5V, ±5%, 500 mW, SOD123, 150°C	MMSZ4693T1G	ON Semi

Mechanical Parts

Item	Qty	Ref Des	Description	MFG Part Number	Manufacturer
1	1	J1	5 Position (1 x 5) header, 0.1 pitch, Vertical	22-28-4050	Molex
2	1	MP1	Board Support, Snap Lock / Screw Mount, Nylon, Length=0.197" (5.00 mm)	702917000	Wurth
3	1	MP2	Board Support, Snap Lock / Screw Mount, Nylon, Length=0.197" (5.00 mm)	702917000	Wurth
4	1	MP3	Board Support, Snap Lock / Screw Mount, Nylon, Length=0.197" (5.00 mm)	702917000	Wurth
5	1	SW1	SWITCH, TOGGLE, SPST, 0.4 VA, 28 V, THD	A11HP	NKK Switches
6	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
7	1	TP2	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
8	1	TP3	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Design Spreadsheet

1	ACDC_LinkSwitchTNZ_Buck_052621; Rev.1.0; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-TNZ Buck
2	**ENTER APPLICATION VARIABLES**					
3	LINE VOLTAGE RANGE			Custom		AC line voltage range
4	VACMIN	90.00		90.00	V	Minimum AC line voltage
5	VACMAX	300.00	Info	300.00	V	The maximum AC line voltage is too high
6	fL	50.00		50.00	Hz	AC mains frequency
7	LINE RECTIFICATION TYPE	H		H		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
8	VOUT	7.00		7.00	V	Output voltage
9	IOUT	0.070		0.070	A	Average output current
10	EFFICIENCY_ESTIMATED	0.70		0.70		Efficiency estimate at output terminals
11	EFFICIENCY_CALCULATED			0.73		Calculated efficiency based on real components and operating point
12	POUT			0.49	W	Continuous output power
13	CIN			2.20	uF	Input capacitor
14	VMIN			74.0	V	Valley voltage of the rectified minimum AC line voltage
15	VMAX			424.3	V	Peak voltage of the maximum AC line voltage
16	INPUT STAGE RESISTANCE	1		1	Ohms	Input stage resistance in ohms (includes thermistor, filtering components, etc)
17	PLOSS_INPUTSTAGE			0.000	W	Maximum input stage loss
21	**ENTER LINKSWITCH-TNZ VARIABLES**					
22	OPERATION MODE			MCM		Mostly continuous mode of operation
23	CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
24	XCAP REQUIRED	NO		NO		Select whether an X-capacitor is required or not
25	PACKAGE			SO-8C		Device package
26	DEVICE SERIES	AUTO		LNK3302		Generic LinkSwitch-TNZ device
27	DEVICE CODE			LNK3302D		Required LinkSwitch-TNZ device
28	ILIMITMIN			0.126	A	Minimum current limit of the device
29	ILIMITTYP			0.136	A	Typical current limit of the device
30	ILIMITMAX			0.146	A	Maximum current limit of the device
31	RDSON			88.40	ohms	Primary switch on-time drain to source resistance at 100degC
32	FSMIN			62000	Hz	Minimum switching frequency
33	FSTYP			66000	Hz	Typical switching frequency
34	FSMAX			70000	Hz	Maximum switching frequency
35	BVDSS			725	V	Device breakdown voltage
39	**SWITCH PARAMETERS**					
40	VDSON			2.00	V	Switch on-time drain to source voltage estimate
41	VDSOFF			445.5	V	Switch off-time drain-to-source voltage stress
42	DUTY			0.107		Maximum duty cycle
43	TIME_ON_MIN			0.688	us	Switch minimum on-time
44	IPED_SWITCH			0.017	A	Maximum switch pedestal current
45	IRMS_SWITCH			0.027	A	Maximum switch RMS current
46	PLOSS_SWITCH			0.081	W	Maximum switch loss
47	THERMAL RESISTANCE OF SWITCH			100	degC/W	Net thermal resistance of the switch
48	T_RISE_SWITCH			8.1	degC	Maximum temperature rise of the switch in degrees Celsius
52	**BUCK INDUCTOR PARAMETERS**					
53	INDUCTANCE_MIN			1980	uH	Minimum design inductance required for current delivery

54	INDUCTANCE_TYP	AUTO		2200	uH	Typical design inductance required for current delivery
55	INDUCTANCE_MAX			2420	uH	Maximum design inductance required for current delivery
56	TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
57	DC RESISTANCE OF INDUCTOR			2.0	ohms	DC resistance of the buck inductor
58	FACTOR_KLOSS			0.50		Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%)
59	IRMS_INDUCTOR			0.092	A	Maximum inductor RMS current
60	PLOSS_INDUCTOR			0.017	W	Maximum inductor losses
64	**FREEWHEELING DIODE PARAMETERS**					
65	VF_FREEWHEELING	0.80		0.80	V	Forward voltage drop across the freewheeling diode
66	PIV_RATING			600.0	V	Peak inverse voltage rating of the freewheeling diode
67	TRR			30	ns	Reverse recovery time of the freewheeling diode
68	PIV_CALCULATED			530.3	V	Computed peak inverse voltage across the freewheeling diode
69	IRMS_DIODE			0.091	A	Maximum diode RMS current
70	PLOSS_DIODE			0.081	W	Maximum freewheeling diode loss
71	RECOMMENDED DIODE			BYV26C		Recommended freewheeling diode
75	**BIAS/FEEDBACK PARAMETERS**					
76	VF_BIAS	0.50		0.50	V	Forward voltage drop of the bias diode
77	RBIAS	40200		40200	Ohms	Bias resistor (connected across FB and S pin). Results into IFB_BIAS value of 49.751 uA
78	RBP			30900	Ohms	BP pin resistor
79	CBP			0.1	uF	BP pin capacitor
80	RFB			53600	Ohms	Feedback resistor
81	CFB			10	uF	Feedback capacitor
82	C_SOFTSTART			N/A	uF	No soft-start capacitor required
83	PLOSS_FEEDBACK			0.001	W	Maximum feedback component losses
87	**X-CAPACITOR DISCHARGE COMPONENTS**					
88	XCAP			N/A	nF	X-capacitor in the input
89	TOLERANCE_RZ	0.05		N/A		Tolerance of the X-capacitor discharge resistors
90	RZ1			N/A	MOhms	X-capacitor discharge resistor connected from the input line to Z1 pin of LinkSwitch-TNZ device
91	RZ2			N/A	MOhms	X-capacitor discharge resistor connected from the input neutral to Z2 pin of LinkSwitch-TNZ device
92	t_XCAP_DISCHARGE			N/A	sec	Actual time (worst-case) to discharge the X-capacitor to 60 V after AC input disconnection
96	**OUTPUT CAPACITOR**					
97	OUTPUT VOLTAGE RIPPLE			140	mV	Desired output voltage ripple
98	IRMS_COUT			0.060	A	Maximum output capacitor RMS current
99	PLOSS_COUT			0.005	W	Maximum output capacitor power loss
100	ESR_COUT			1329	mOhms	ESR of the output capacitor

8 Performance Data

8.1 *Full Load Efficiency*

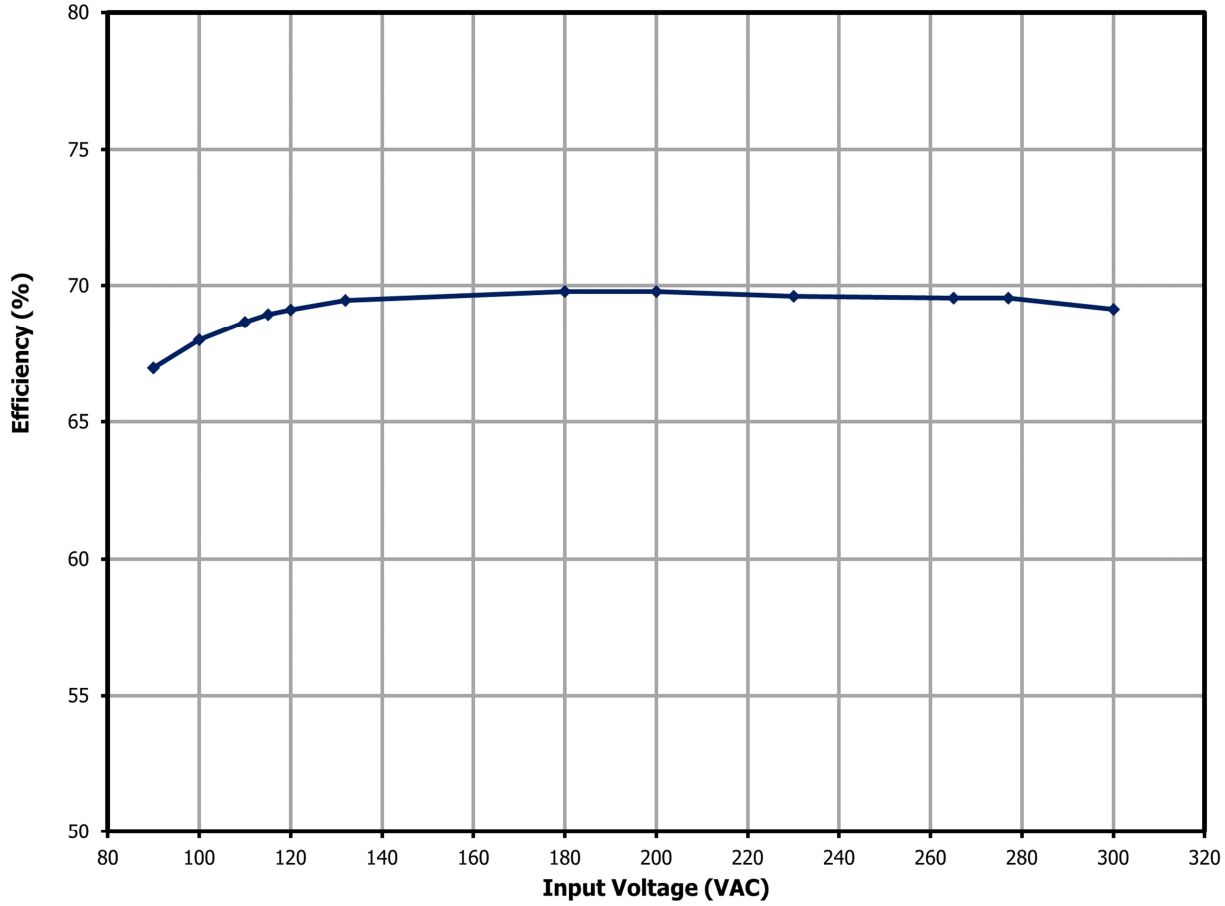

Figure 12 – Full Load Efficiency vs. Line.

8.2 *Efficiency vs Load*

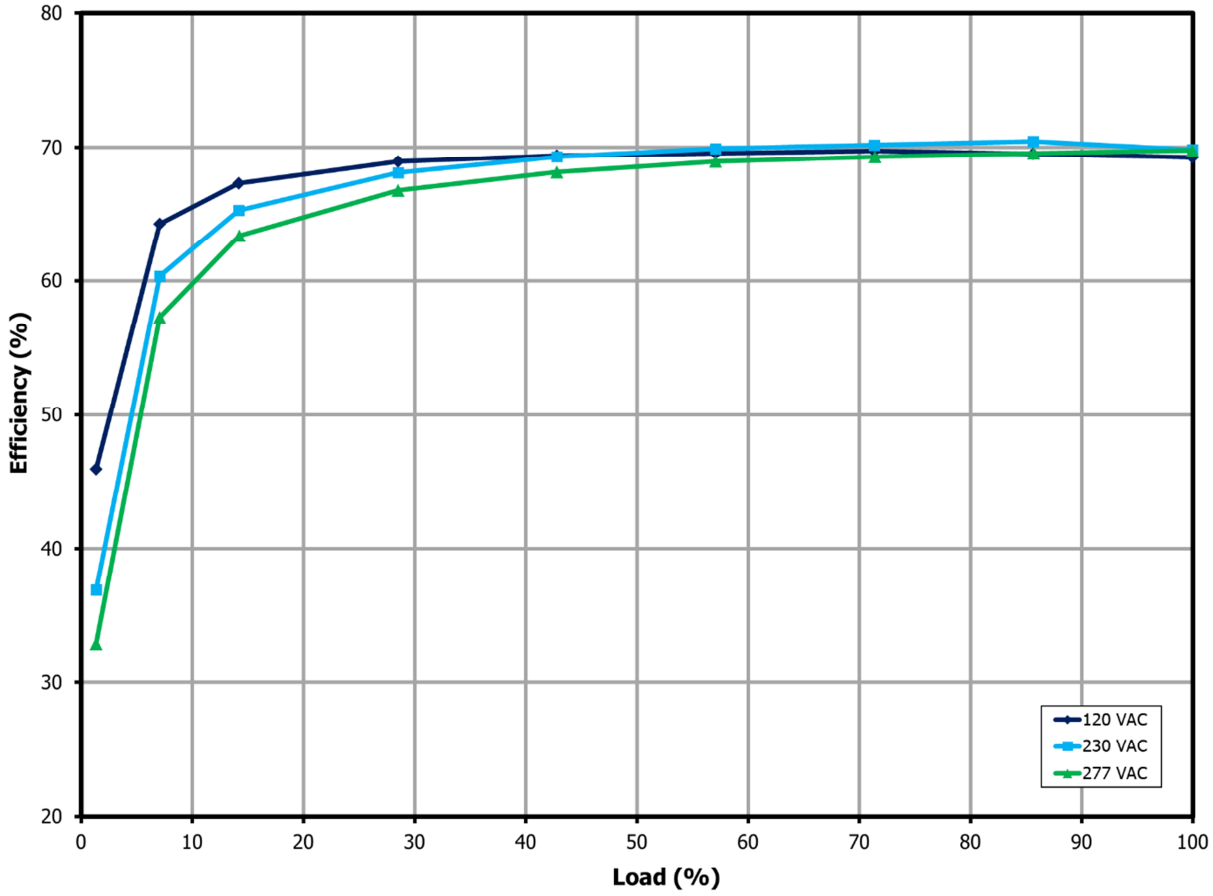

Figure 13 – Full Load Efficiency vs. Load.

8.3 *Line Regulation*

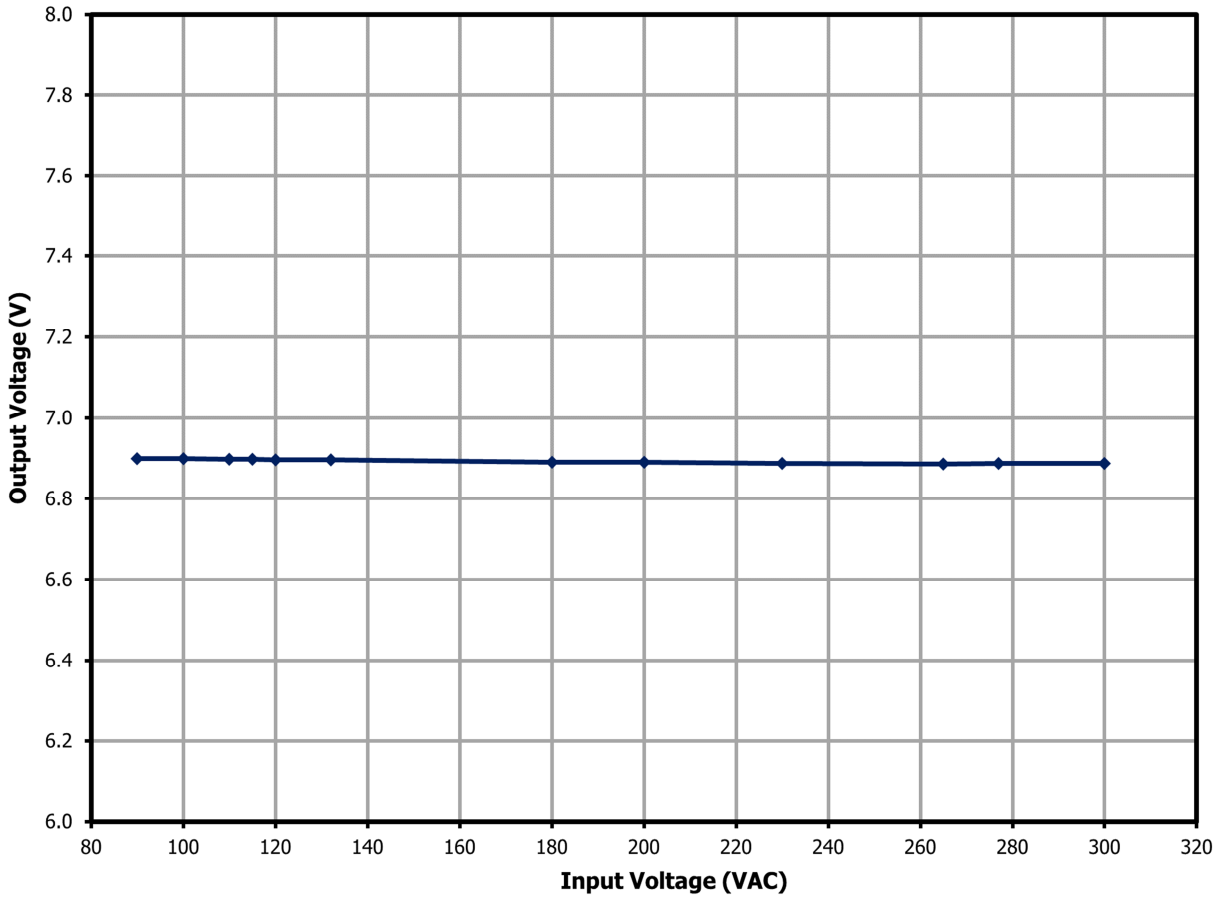

Figure 14 – Output Voltage vs. Line Voltage.

8.4 *Load Regulation*

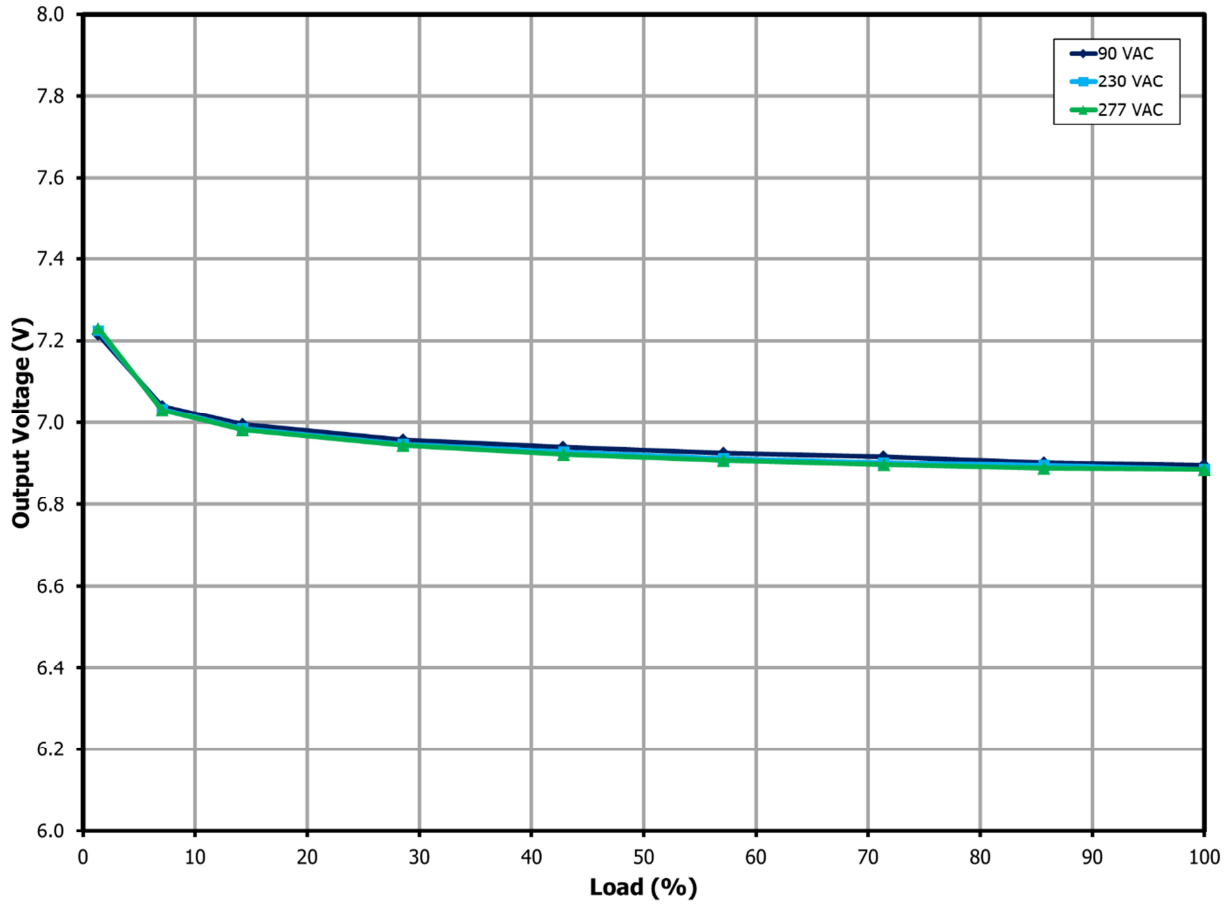

Figure 15 – Output Voltage vs. Percent Load.

8.5 *Standby Input Current*

Test Condition: Soak for 5 minutes each line and use Fluke DMM.

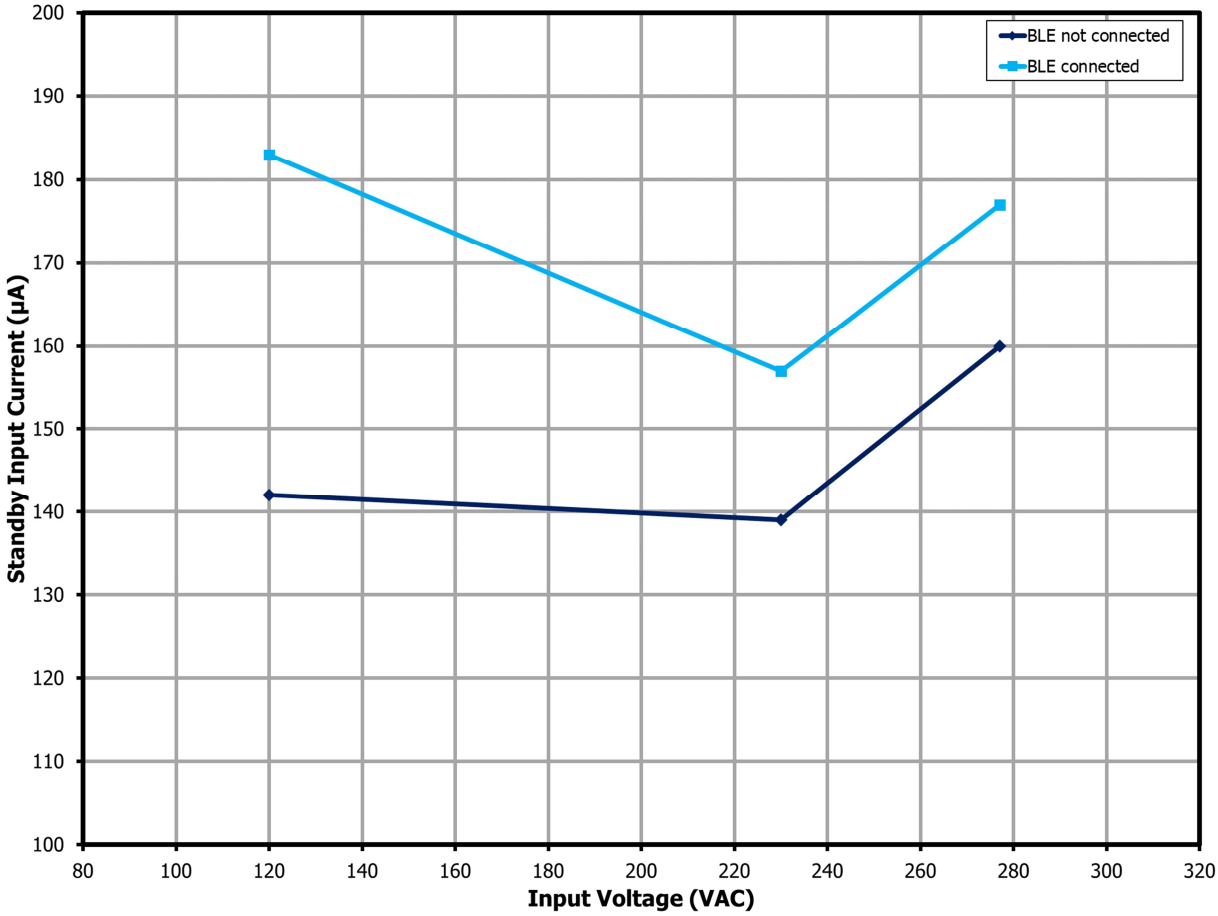

Figure 16 – No-Load Input Current vs. Line.

9 Electrical Test Data

9.1 *Full Load Line Regulation and Efficiency*

Input		Input Measurement				Output Measurement				
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
90	60	90.01	13.63	0.72	0.59	6.90	69.98	0.48	-1.43	66.98
100	60	99.96	12.55	0.71	0.57	6.90	69.98	0.48	-1.44	68.00
110	60	110.00	11.69	0.70	0.55	6.90	69.98	0.48	-1.46	68.66
115	60	114.98	11.31	0.70	0.54	6.90	69.98	0.48	-1.46	68.94
120	60	119.95	10.98	0.70	0.53	6.90	69.98	0.48	-1.47	69.11
132	60	131.96	10.28	0.69	0.51	6.90	69.98	0.48	-1.49	69.46
180	50	179.98	8.26	0.69	0.46	6.89	69.97	0.48	-1.56	69.79
200	50	199.96	7.72	0.69	0.45	6.89	69.97	0.48	-1.57	69.78
230	50	229.98	7.06	0.69	0.43	6.89	69.97	0.48	-1.61	69.62
265	50	264.99	6.44	0.69	0.41	6.89	69.97	0.48	-1.63	69.56
277	60	277.04	6.30	0.69	0.40	6.89	69.97	0.48	-1.60	69.56
300	60	300.11	6.00	0.70	0.39	6.89	69.97	0.48	-1.60	69.14

9.2 *Load Regulation and Efficiency*

9.2.1 120 VAC

	Input		Input Measurement				Output Measurement				
% Load	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
100	120	60	119.95	10.94	0.70	0.53	6.90	69.96	0.48	-1.49	69.26
86	120	60	119.95	9.60	0.60	0.52	6.90	59.96	0.41	-1.40	69.51
71	120	60	119.95	8.23	0.50	0.50	6.92	49.96	0.35	-1.19	69.76
57	120	60	119.95	6.84	0.40	0.48	6.93	39.95	0.28	-1.06	69.58
43	120	60	119.95	5.39	0.30	0.46	6.94	29.97	0.21	-0.86	69.39
29	120	60	119.95	3.83	0.20	0.44	6.96	19.95	0.14	-0.60	68.93
14	120	60	119.95	2.12	0.10	0.41	7.00	9.95	0.07	-0.07	67.28
7	120	60	119.95	1.14	0.05	0.39	7.04	4.95	0.03	0.59	64.24
1	120	60	119.95	0.27	0.01	0.45	7.22	0.94	0.01	3.07	45.93

9.2.2 230 VAC

	Input		Input Measurement				Output Measurement				
% Load	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
100	230	50	229.98	7.03	0.69	0.43	6.89	69.97	0.48	-1.63	69.83
86	230	50	229.98	6.14	0.59	0.42	6.90	59.96	0.41	-1.47	70.47
71	230	50	229.98	5.28	0.49	0.40	6.90	49.96	0.34	-1.39	70.20
57	230	50	229.98	4.39	0.40	0.39	6.91	39.96	0.28	-1.24	69.91
43	230	50	229.98	3.45	0.30	0.38	6.93	29.97	0.21	-1.03	69.31
29	230	50	229.98	2.45	0.20	0.36	6.95	19.95	0.14	-0.76	68.08
14	230	50	229.98	1.35	0.11	0.34	6.99	9.95	0.07	-0.21	65.25
7	230	50	229.98	0.73	0.06	0.34	7.03	4.95	0.03	0.47	60.33
1	230	50	229.98	0.23	0.02	0.36	7.23	0.95	0.01	3.23	36.92

9.2.3 277 VAC

	Input		Input Measurement				Output Measurement				
% Load	VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	PF	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
100	277	60	277.03	6.28	0.69	0.40	6.89	69.97	0.48	-1.61	69.79
86	277	60	277.04	5.52	0.59	0.39	6.89	59.97	0.41	-1.59	69.55
71	277	60	277.03	4.74	0.50	0.38	6.90	49.97	0.34	-1.46	69.29
57	277	60	277.03	3.93	0.40	0.37	6.91	39.96	0.28	-1.31	68.97
43	277	60	277.03	3.09	0.30	0.36	6.92	29.97	0.21	-1.10	68.17
29	277	60	277.03	2.19	0.21	0.34	6.94	19.96	0.14	-0.80	66.79
14	277	60	277.03	1.21	0.11	0.33	6.98	9.95	0.07	-0.26	63.35
7	277	60	277.04	0.66	0.06	0.33	7.03	4.95	0.03	0.44	57.25
1	277	60	277.03	0.23	0.02	0.33	7.23	0.95	0.01	3.30	32.94

9.3 ***Standby Input Current***

Input (VAC)	BLE disconnected (µA)	BLE connected (µA)
120	142	183
230	139	157
277	160	177

10 Waveforms

10.1 *Drain Voltage and Current*

10.1.1 Drain Voltage and Current at Start-up

Figure 17 – 90 VAC 60 Hz.
CH2: V_{DRAIN}, 100 V / div., 5 ms / div.
CH4: I_{DRAIN}, 100 mA / div., 5 ms / div.
$V_{DRAIN(PEAK)}$: 127 V; $I_{DRAIN(PEAK)}$: 293 mA.

Figure 18 – 300 VAC 60 Hz.
CH2: V_{DRAIN}, 100 V / div., 5 ms / div.
CH4: I_{DRAIN}, 100 mA / div., 5 ms / div.
$V_{DRAIN(PEAK)}$: 432 V; $I_{DRAIN(PEAK)}$: 420 mA.

10.1.2 Drain Voltage and Current at Normal Operation

Figure 19 – 90 VAC 60 Hz.
CH2: V_{DRAIN}, 100 V / div., 2 ms / div.
CH4: I_{DRAIN}, 100 mA / div., 2 ms / div.
$V_{DRAIN(PEAK)}$: 127 V; $I_{DRAIN(PEAK)}$: 144 mA.

Figure 20 – 300 VAC 60 Hz.
CH2: V_{DRAIN}, 100 V / div., 2 ms / div.
CH4: I_{DRAIN}, 100 mA / div., 2 ms / div.
$V_{DRAIN(PEAK)}$: 432 V; $I_{DRAIN(PEAK)}$: 177 mA.

10.1.3 Drain Voltage and Current at Start-up, Shorted Output

Figure 21 – 90 VAC 60 Hz.
CH2: $V_{DRAIN,}$ 100 V / div., 5 ms / div.
CH4: $I_{DRAIN,}$ 100 mA / div., 5 ms / div.
$V_{DRAIN(PEAK)}$: 127 V; $I_{DRAIN(PEAK)}$: 293 mA.

Figure 22 – 300 VAC 60 Hz.
CH2: $V_{DRAIN,}$ 100 V / div., 5 ms / div.
CH4: $I_{DRAIN,}$ 100 mA / div., 5 ms / div.
$V_{DRAIN(PEAK)}$: 422 V; $I_{DRAIN(PEAK)}$: 403 mA.

10.1.4 Drain Voltage and Current, Shorted Output During Normal Operation

Figure 23 – 90 VAC 60 Hz.
CH2: $V_{DRAIN,}$ 100 V / div., 500 ms / div.
CH4: $I_{DRAIN,}$ 100 mA / div., 500 ms / div.
$V_{DRAIN(PEAK)}$: 127 V; $I_{DRAIN(PEAK)}$: 224 mA.

Figure 24 – 300 VAC 60 Hz.
CH2: $V_{DRAIN,}$ 100 V / div., 500 ms / div.
CH4: $I_{DRAIN,}$ 100 mA / div., 500 ms / div.
$V_{DRAIN(PEAK)}$: 432 V; $I_{DRAIN(PEAK)}$: 383 mA.

10.2 *Output Voltage and Current at Full-load Start-up*

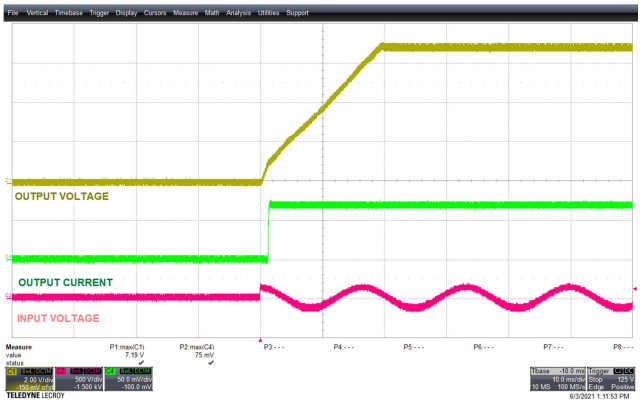

Figure 25 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.19 V.

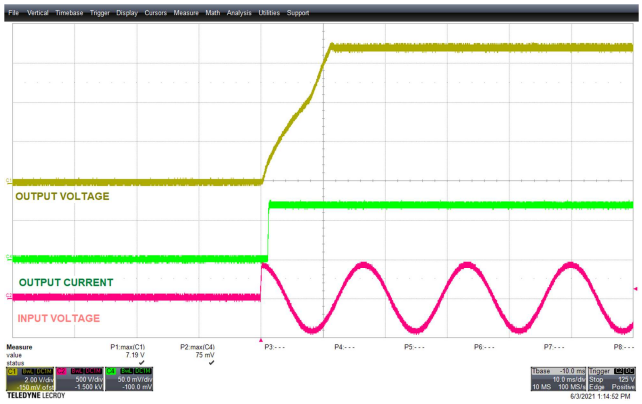

Figure 26 – 300 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.19 V.

10.3 *Output Voltage and Current at 0.1 mA Load Start-up*

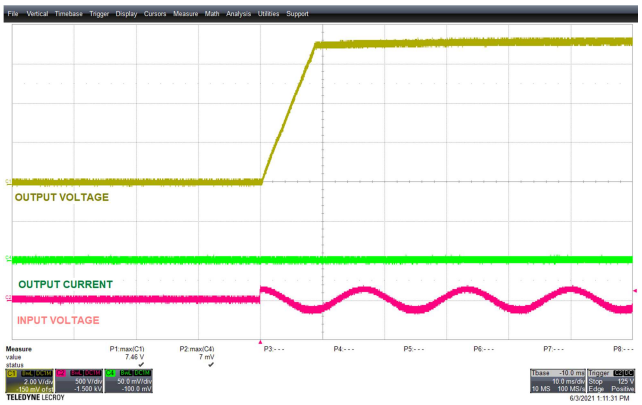

Figure 27 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.46 V.

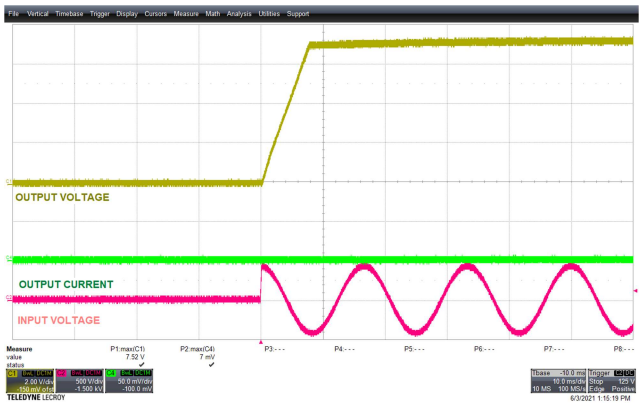

Figure 28 – 300 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.52 V.

10.4 *Output Voltage and Current at Full-load, Output Short and Recovery*

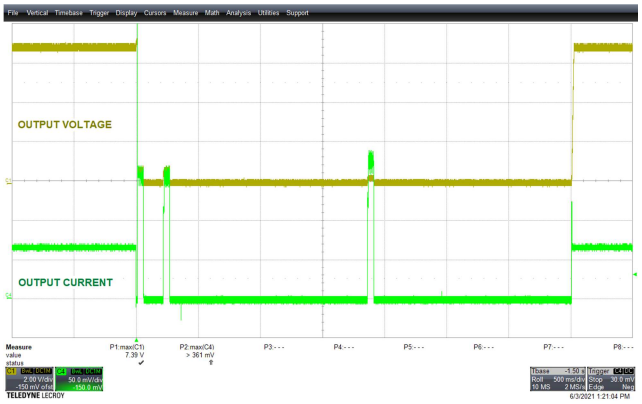

Figure 29 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.39 V.

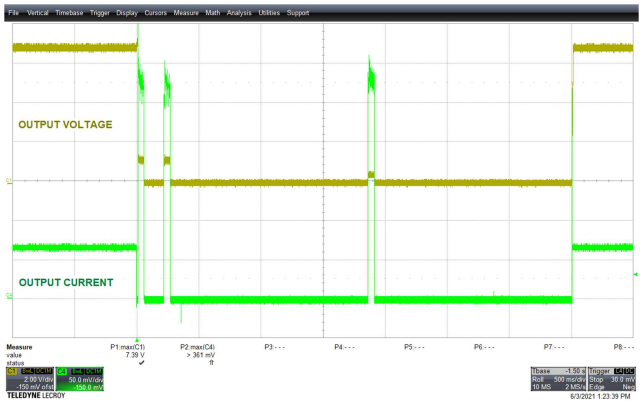

Figure 30 – 300 VAC 60 Hz.
CH1: $V_{OUT,}$ 2 V / div., 10 ms / div.
CH2: $V_{IN,}$ 500 V / div., 10 ms / div.
CH4: $I_{OUT,}$ 50 mA / div., 10 ms / div.
$V_{OUT(PEAK)}$: 7.39 V.

10.5 *Zero-Crossing Detection*

10.6 *Conduction Angle*

10.6.1 Leading-edge Mode, Incandescent Bulb Load, 120 VAC, 60 Hz

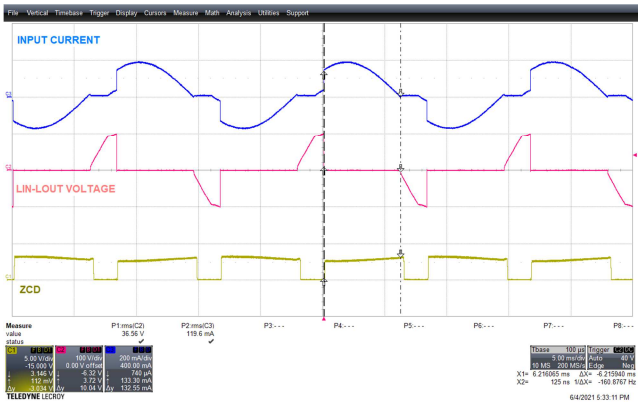

Figure 31 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT,}$ 100 V / div., 5 ms / div.
CH3: $I_{IN,}$ 200 mA / div., 5 ms / div.
Maximum Conduction Time: 6.22 ms (134 °).

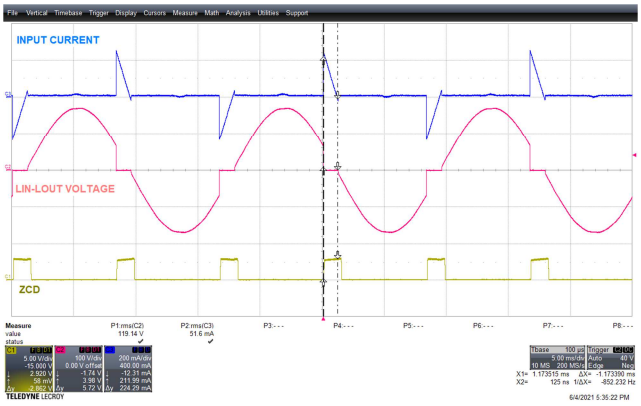

Figure 32 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT,}$ 100 V / div., 5 ms / div.
CH3: $I_{IN,}$ 200 mA / div., 5 ms / div.
Maximum Conduction Time: 1.17 ms (25 °).

10.6.2 Leading-edge Mode, Incandescent Bulb Load, 230 VAC, 50 Hz

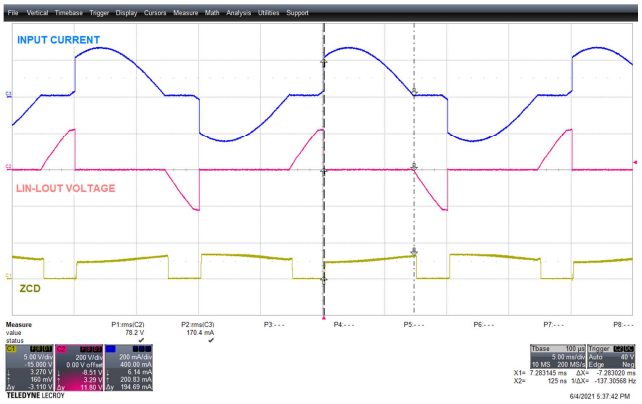

Figure 33 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 7.28 ms (131 °).

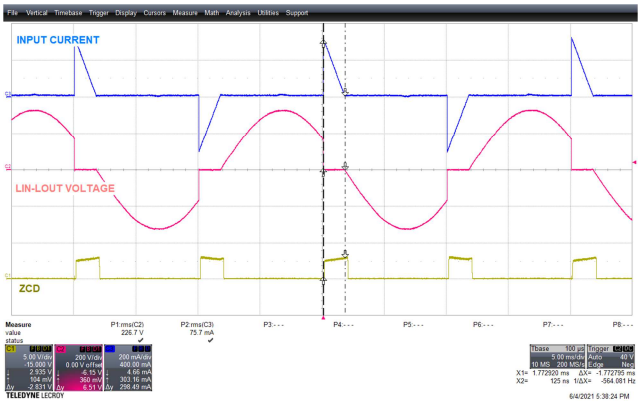

Figure 34 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 1.77 ms (32 °).

10.6.3 Trailing-edge Mode, Incandescent Bulb Load, 120 VAC, 60 Hz

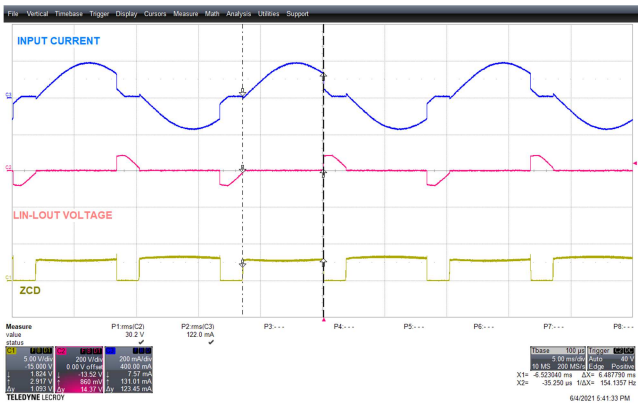

Figure 35 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 6.49 ms (140 °).

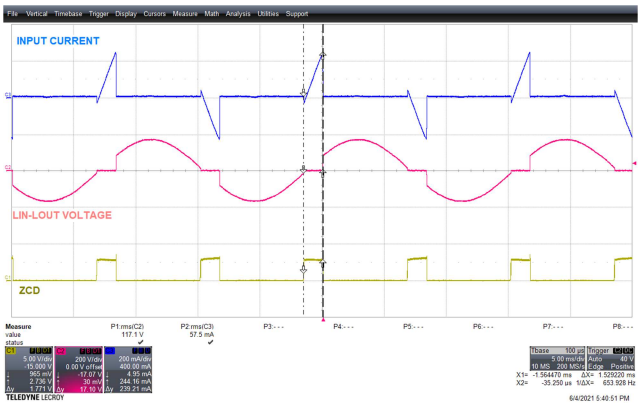

Figure 36 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 1.56 ms (34 °).

10.6.4 Trailing-edge Mode, Incandescent Bulb Load, 230 VAC, 50 Hz

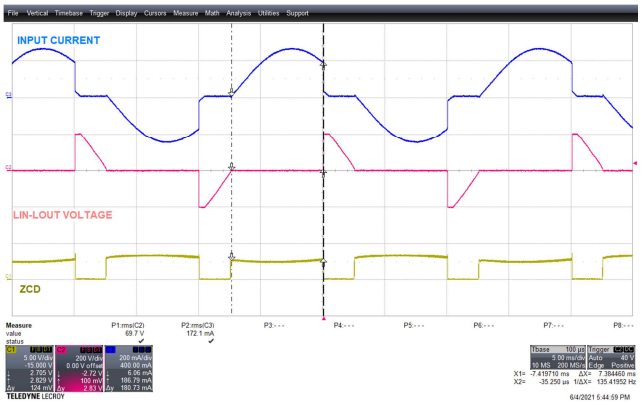

Figure 37 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 7.42 ms (133 °).

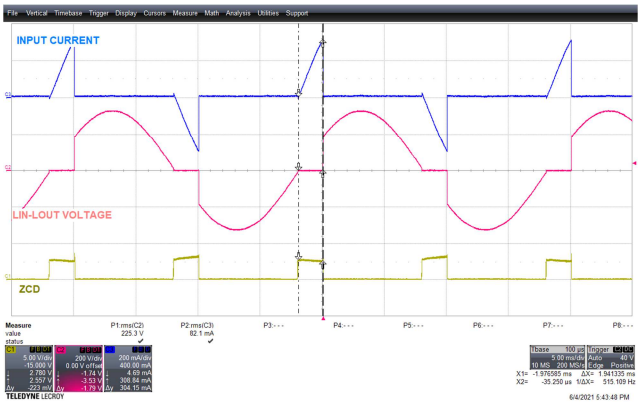

Figure 38 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{LIN-LOUT}$, 100 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Maximum Conduction Time: 1.98 ms (35 °).

10.7 ***Zero Crossing Detection Delay***

10.7.1 Leading-edge Mode

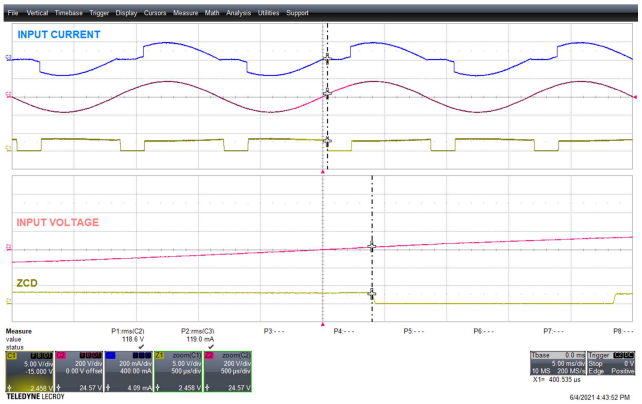

Figure 39 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 200 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Falling-edge Delay: 400 µs.

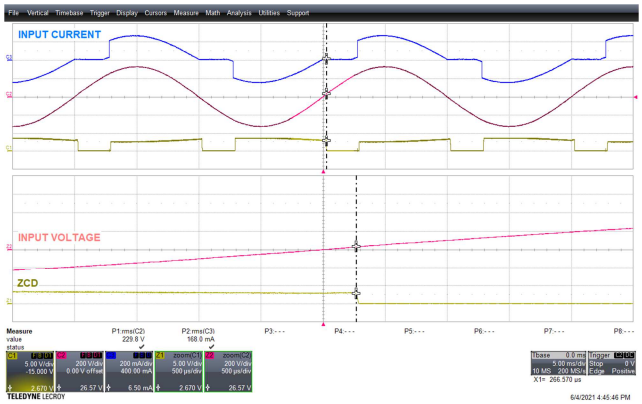

Figure 40 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 200 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Falling-edge Delay: 266 µs.

10.7.1 Trailing-edge Mode

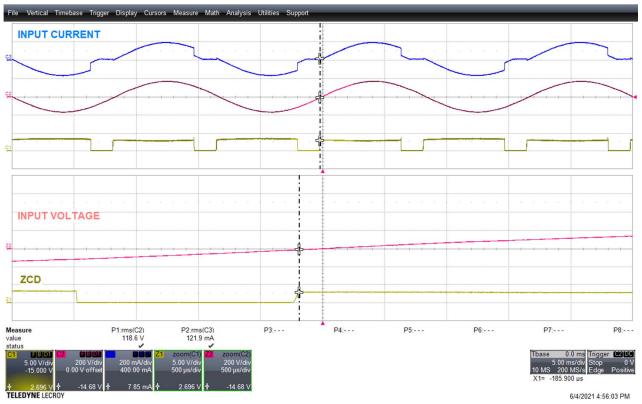

Figure 41 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 200 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Rising-edge Delay: -186 µs.

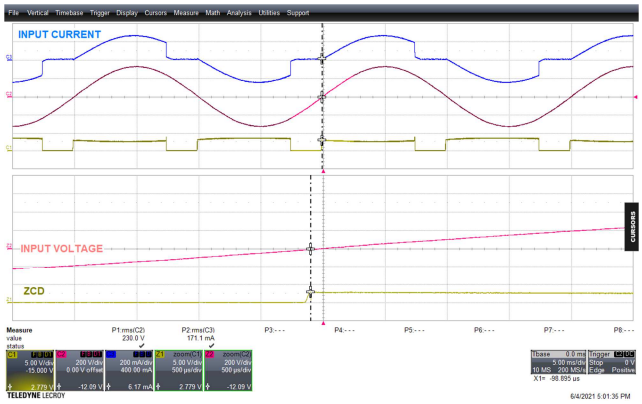

Figure 42 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 200 V / div., 5 ms / div.
CH3: I_{IN}, 200 mA / div., 5 ms / div.
Rising-edge Delay: -99 µs.

11 Thermal Performance

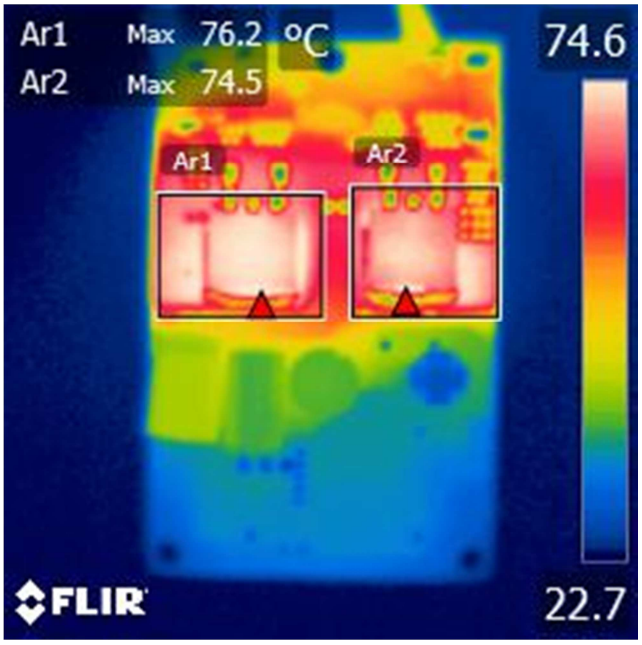

Figure 43 – 120 VAC 60 Hz, 250 W Synthetic Low PF Load, Top.
Ar1: Q2, 76.2 °C.
Ar2: Q6, 74.5 °C.

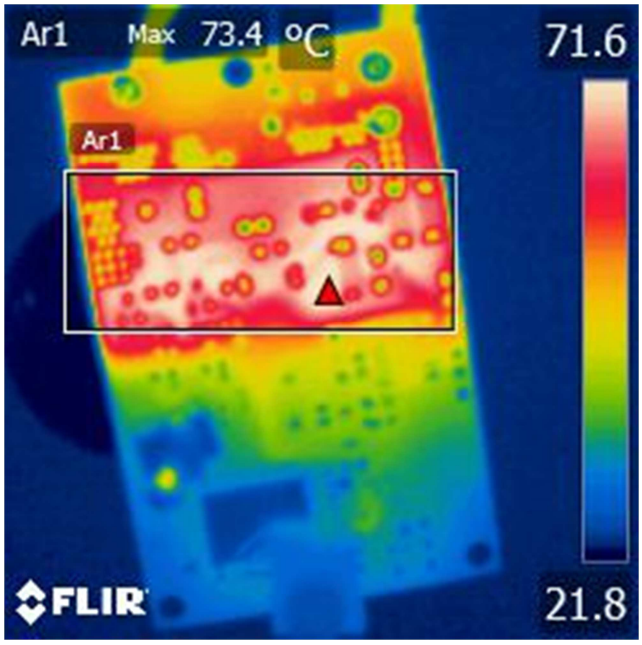

Figure 44 – 120 VAC 60 Hz, 250 W Synthetic Low PF Load, Bottom.
Ar1: 73.4 °C.

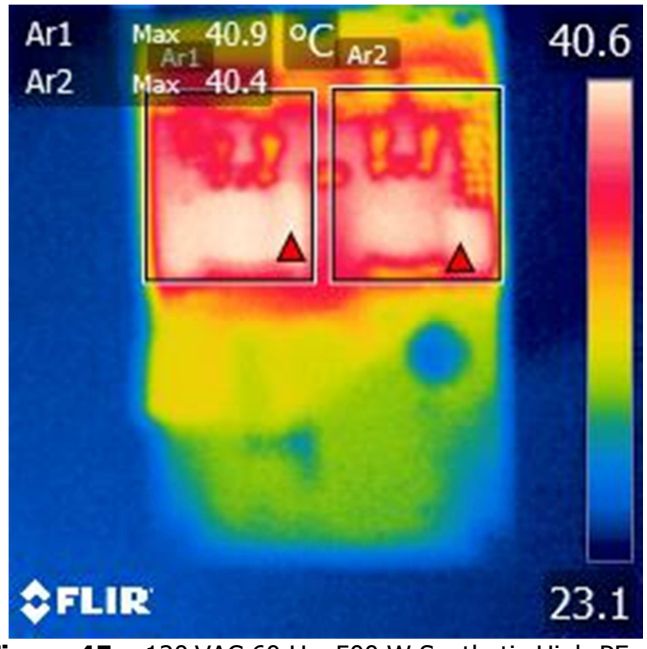

Figure 45 – 120 VAC 60 Hz, 500 W Synthetic High-PF Load, Top.
Ar1: Q2, 40.9 °C.
Ar2: Q6, 40.4 °C.

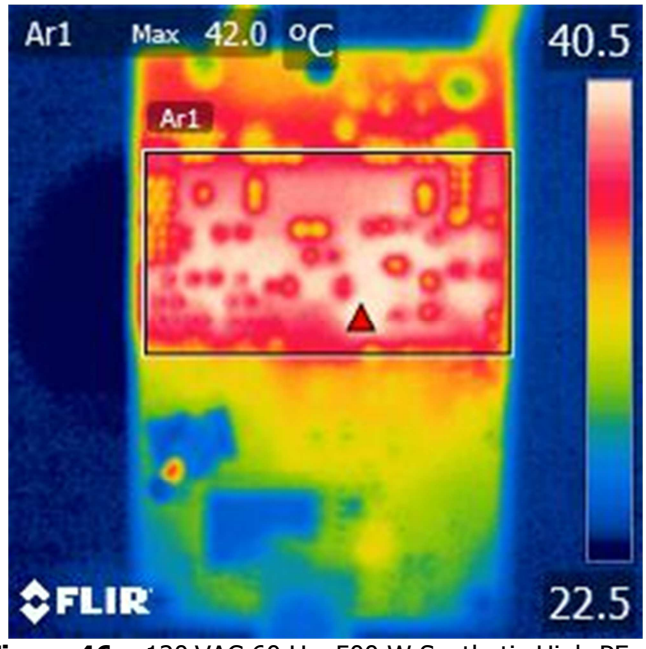

Figure 46 – 120 VAC 60 Hz, 500 W Synthetic High-PF Load, Bottom.
Ar1: 42 °C.

12 Conclusted EMI

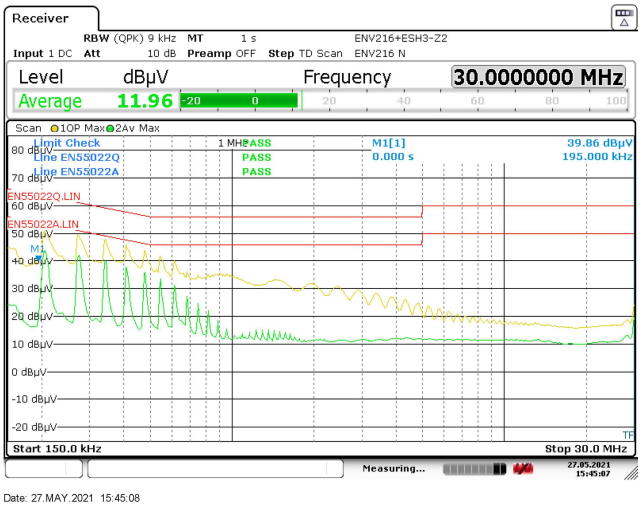

Figure 47 – 115 VAC 60 Hz.

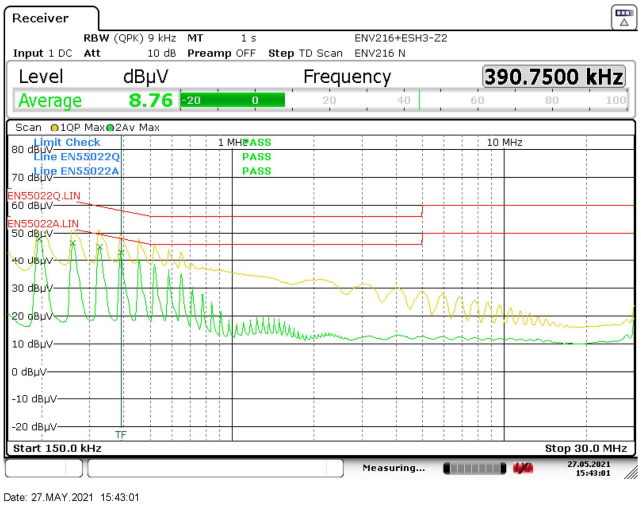

Figure 48 – 230 VAC 60 Hz.

13 Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was in Light-OFF mode during the surge event.

13.1 *Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

13.2 *Ring Wave*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
+2500	230	L to N	180	Pass
-2500	230	L to N	180	Pass
+2500	230	L to N	270	Pass
-2500	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
22-Jun-21	DS	1.0	Initial Release.	Apps & Mktg
23-Jul-21	KM	1.1	Minor Formatting Change.	Mktg

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