

Rapidly Implement Application Circuits Up to 8 W Using CamSemi's PSS Topology and Advanced Controller ICs

C2161PX2 (SOT23-6) C2162PX2 (SOT23-6)

CamSemi's PSS topology and advanced controller ICs deliver low cost solutions for flyback power supply applications such as mobile phone chargers, xDSL modems, USB chargers, handheld gaming consoles, wireless headsets, cordless phone chargers, etc, where accurate control of output voltage and output current limit are required.

By fixing some design parameters, this guide enables users to rapidly create a working prototype with rated nominal output up to 8 W and characteristics as shown in Figure 2. Components are selected from simple lookup tables and charts, and transformer construction is explained. Other design guides or application notes explain how solutions can be optimised to meet particular application requirements. To obtain these guides and the controller IC datasheet (reference DS-2918) please contact your CamSemi representative.

The application schematic configuration required depends on two main parameters as shown in Figure 1. Using this guide, the user can select component values to create a power supply design, with chosen input voltage, power rating and output voltage. CamSemi controller IC selection is covered in section 2.4.1.

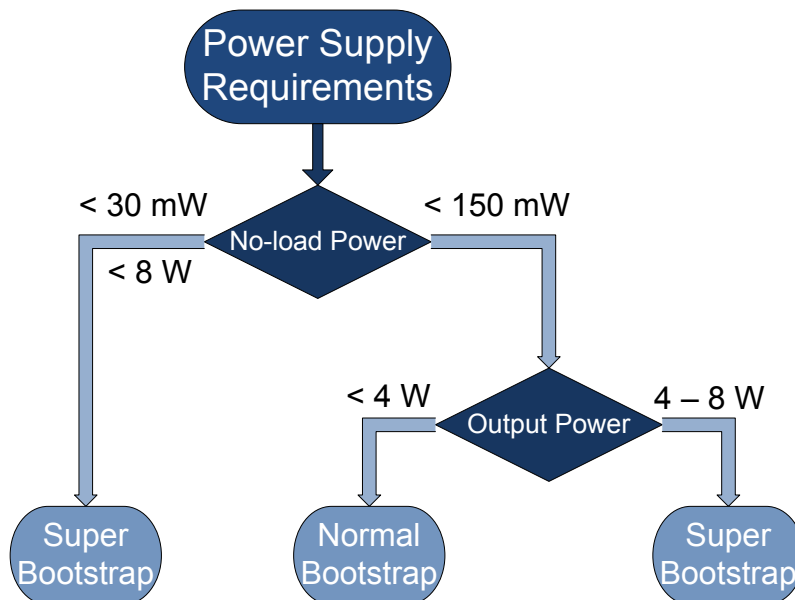


Figure 1: Schematic Configuration Decision Tree

A worked PSS design example is described in section 7.

Contents

1	APPLICATION DESIGN PARAMETERS	3
1.1	Output Characteristic	4
2	GENERAL COMPONENT SELECTION	5
2.1	Input Rectifier and Filter	6
2.2	Switch Component	8
2.3	Transformer Design.....	9
2.4	Controller Components	14
2.5	Feedback Components	17
2.6	Current Sense Components.....	18
2.7	VDD and Auxiliary Components.....	19
2.8	Output Components	22
2.9	Minimising the Bill of Materials.....	26
3	NORMAL BOOTSTRAP OPTION	27
3.1	Base Diode (Dbase).....	27
3.2	Start-up Resistors (Rht, or Rht1 and Rht2).....	27
3.3	Base Resistor (Rbase).....	28
4	SUPER BOOTSTRAP OPTION	29
5	ENHANCEMENTS	31
5.1	Alternative Rcs Arrangement (Rcso1, Rcso2, Rcso3).....	31
5.2	Reduced Output Voltage Ripple Option (Csfilt, Lsfilt).....	32
5.3	Reduced Collector Voltage Option (Rpsnub1, Rpsnub2, Cpsnub, Dpsnub)	33
5.4	Simplified Transformer Design for 1-3 W Applications	34
6	TESTING AND TROUBLESHOOTING YOUR DESIGN	35
6.1	Safety	35
6.2	First Power-up (100% Load)	36
6.3	Typical Controller Waveforms	36
6.4	Troubleshooting.....	37
7	EXAMPLE APPLICATION DESIGN	39
7.1	Application Design Parameters.....	39
7.2	Components Selected Using Design Guide.....	40
7.3	Measured Performance.....	42
7.4	Voltage Ripple	48
APPENDIX A	DESIGN WORKSHEET	52
A.1	Specify Your Design Parameters	52
A.2	Select Components Using Design Guide.....	53
A.3	Measure Performance of Your Design.....	54

1 APPLICATION DESIGN PARAMETERS

Table 1 lists key application design parameters. It provides an indication of performance achievable with the PSS topology in general and, in particular, when using this design guide. Design parameters that are specified by the user when using this guide are shown as “User Defined”.

Design Parameter	Symbol	Typical Range Achievable	Design Guide Typical Value	Comments
Nominal output power	P_{NOM}	2 to 8 W	User Defined	Range supported
Nominal output voltage	V_{NOM}	3 to 24 V	User Defined ¹	CV mode
Nominal output current	I_{NOM}	0.1 to 2.5 A	P_{NOM} / V_{NOM}	Constrains allowable P_{NOM} , V_{NOM}
Output voltage tolerance	K_{CVTOL}	< 10%	10%	CV mode
Output current tolerance	K_{CCTOL}	< 15%	10%	
Cable compensation	G_{CAB}	2 to 10%	User Defined ²	
Nominal switching frequency at full load	F_{NOM}	40 to 65 kHz	User Defined	Component adjustments required to achieve target
Input voltage	V_{AC}	85 to 265 Vac	85 to 265 Vac	Universal input
Input voltage frequency	F_{AC}	45 to 66 Hz	50/60 Hz	
Input voltage withstand		0 to 85 Vac and 265 to 300 Vac	0 to 85 Vac and 265 to 300 Vac	
Rectified input voltage	V_{DC}	80 V to 375 V	70 V to 375 V	$V_{DC(MIN)}$, when applied to converter supplying P_{NOM} , will generate a duty cycle of 0.50
Average system efficiency	η_{NOM}	63% to 85%	EPS 2.0 (Level V) / EU CoC V4	Low power, low output voltage applications will be less efficient
No-load power consumption	P_{NL}	< 150 mW	Four Star / EU CoC V4	Normal or Super Bootstrap
		< 30 mW	Five Star	Super Bootstrap
Transformer inductance tolerance	K_{LPTOL}	0 to $\pm 15\%$	10%	
Conducted emissions EN55022 class B	-	Compliant with margin	Compliant with 6 dB margin	High power may require snubber and careful transformer design
Maximum duty cycle	D_{MAX}	50%-60%	50%	
Nominal duty cycle	D_{NOM}	Defined by D_{MAX}	45%	Assuming K_{LPTOL} is 10%
DC brown-out voltage	V_{DCBRN}	65 V to 75 V	70 V	
Auxiliary voltage	V_{AUX}	4 V to 5 V	4 V	At no-load
Q1 turn-off time	t_{BJTOFF}	100 ns to 400 ns	200 ns	BJT storage time
Output diode forward voltage	V_{DF}	0.25 V (schottky) 0.65 V (epitaxial)	0.25 V	
Transformer resonance frequency (in-circuit)	F_{RES}	> 300 kHz	400 kHz	
Feedback adjustment factor	t_{FB}	70 ns	70 ns	

Table 1: Key Application Design Parameters

¹Generally a nominal output voltage of 5 V is assumed. Formulae to calculate for other output voltages are given. Alternative example output voltages are given for transformer design and feedback resistor selection.

²Generally a required cable compensation of 5% is assumed. Formulae to calculate for other cable compensations are given.

1.1 Output Characteristic

The output voltage-current characteristics are defined in Figure 2. Figure 3 shows the VI mask parameters. Trade-offs between parameters may be necessary.

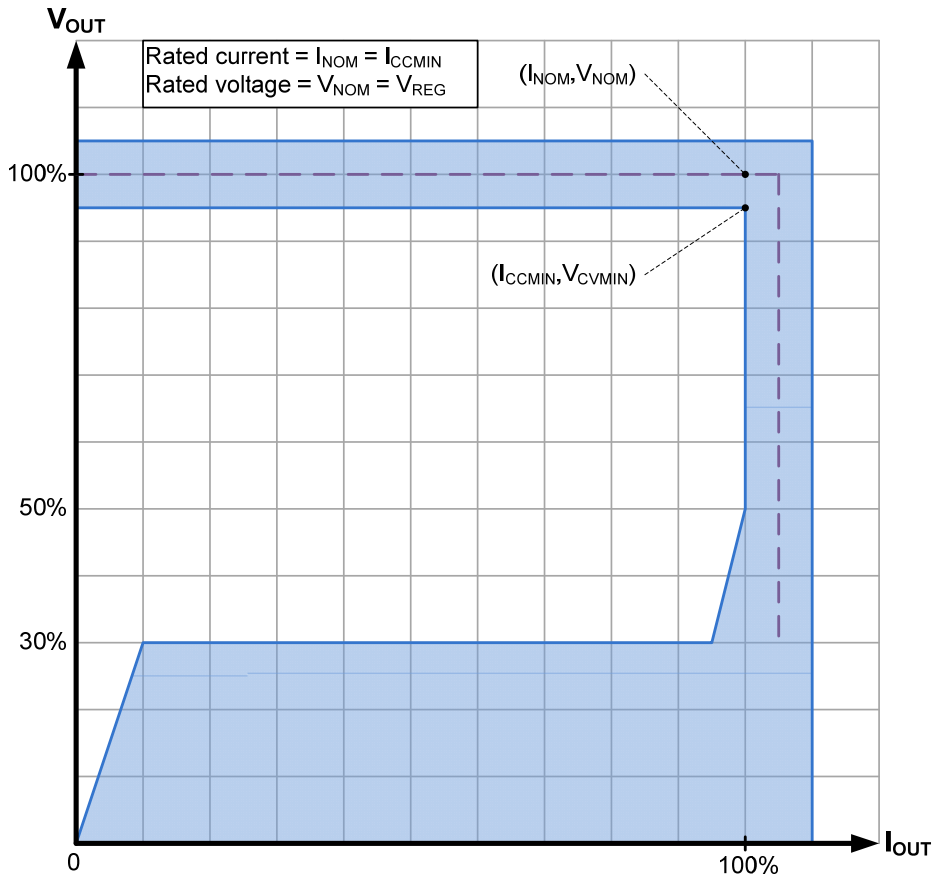


Figure 2: Output VI Characteristic

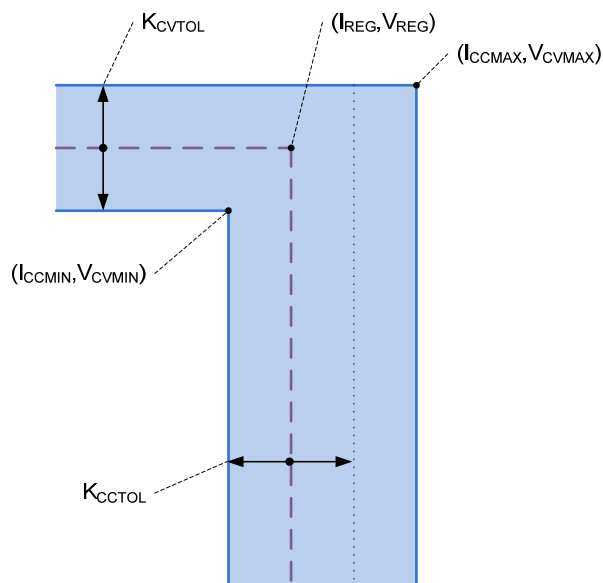


Figure 3: VI Mask - Parametric Details

2 GENERAL COMPONENT SELECTION

Figure 1 illustrates a typical PSS application circuit. This section details the selection of the majority of components for the application; the highlighted components in the schematic are covered.

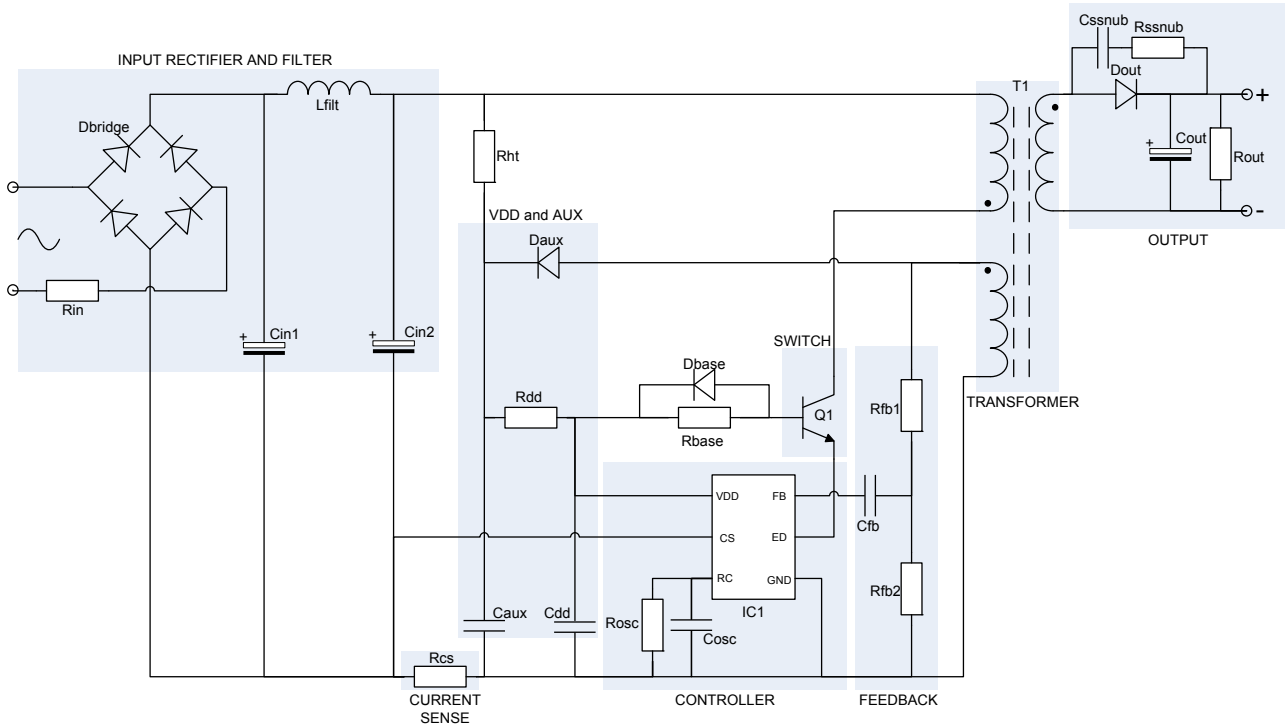


Figure 4: Typical PSS Application Circuit

Note the schematic shown is a normal bootstrap configuration. The other normal bootstrap configuration components are covered in section 3. The alternative super bootstrap configuration components are covered in section 4.

Table 2 lists the components in a typical application circuit as shown in Figure 4. Some values and types are fixed for designs that can be created with this guide. Others will be determined by working through the guide (in the sections referenced in the “Type / Value” column).

Lookup tables in this design guide may not have an exact match for a parameter value required in your target application. In such cases, interpolate between the two values adjacent to the desired value for your design.

Block	Components	Type / Value	Function
Input Rectifier and Filter	Dbridge	See section 2.1.1	Full wave rectification of the ac input voltage and reduction of line frequency ripple and differential mode EMI (by virtue of the pi filter behaviour)
	Rin	See section 2.1.2	
	Lfilt	See section 2.1.3	
	Cin1	See section 2.1.4	
	Cin2	See section 2.1.4	
Switch	Q1	See section 2.2.1	Power Switch
Transformer	T1	See section 2.3	Isolation barrier and flyback power conversion
Controller	IC1	See section 2.4.1	PSS mode converter controller and frequency setting components
	Cosc	See section 2.4.2	
	Rosc	See section 2.4.2	
Feedback	Rfb1	See section 2.5.1	Voltage feedback loop
	Rfb2	See section 2.5.1	
	Cfb	See section 2.5.2	
Current Sense	Rcs	See section 2.6.1	Current sense and offset
VDD and Auxiliary	Caux	See section 2.7.1	Initial start-up and auxiliary power supply
	Daux	See section 2.7.2	
	Cdd	See section 2.7.3	
	Rdd	See section 2.7.4	
Output	Dout	See section 2.8.1	Secondary voltage rectification and filtering
	Cout	See section 2.8.2	
	Rout	See section 2.8.3	
	Cssnub	See section 2.8.4	
	Rssnub	See section 2.8.4	

Table 2: Application Circuit Components

2.1 Input Rectifier and Filter

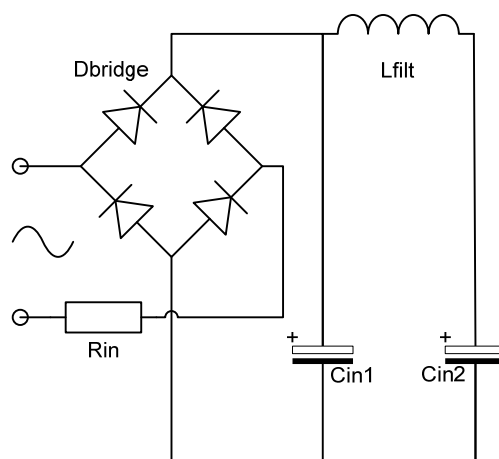


Figure 5: Input Rectifier and Filter Components

2.1.1 Input Line Rectifier (Dbridge)

The input line rectifier can be implemented with four discrete diodes or an integrated bridge rectifier depending on the power requirement, cost and PCB area available for the application. A DB106 bridge rectifier or four 1N4007 diodes are preferred but any other diodes with the following can be used:

- Repetitive reverse maximum voltage rating, $V_{RRM} > 600 \text{ V}$
- Average forward current rating, $I_{F(AV)} > 1 \text{ A}$
- Surge forward current rating, $I_{F(SURGE)} > 25 \text{ A}$

2.1.2 Inrush Limiter Resistor (Rin)

Rin limits the current during power-up and surge. The value of Rin is best found empirically to keep inrush current $< 25 \text{ A}$ (peak). Typical Rin selection is 10Ω .

2.1.3 Input Filter (Lfilt)

The input filter can be a fixed value of $330 \mu\text{H}$.

A full explanation and calculation of the circuit noise sources is outside the range of this design guide, but it should be noted that it might be necessary to increase this value to compensate for differential noise. This can be done through trial and error. It is important to be aware of the current rating and temperature rating of the inductor, and ensure that the inductor does not saturate.

2.1.4 Input Capacitors (Cin1 and Cin2)

The input capacitors aim to hold the rectified supply voltage above a brown-out level. The capacitors are placed in a π filter arrangement with a series inductor (Lfilt). The combined capacitance holds the rectified supply above the brown-out level.

The following table assumes a brown-out level (V_{DCBRN}) of 70 V , and a low mains switching efficiency (η_{SWLV}) of 90% . The capacitor values in the table have been rounded up to the nearest E6 value. The capacitors require a voltage rating of 400 V .

AC(MIN)	85 Vac / 45 Hz			90 Vac / 50 Hz		
P _{NOM} (W)	Cin1 (μF)	Cin2 (μF)	Min Total	Cin1 (μF)	Cin2 (μF)	Min Total
1	1	2.2	1.8	1	1	1.4
2	2.2	3.3	3.6	2.2	2.2	2.9
3	3.3	4.7	5.4	2.2	3.3	4.3
4	4.7	4.7	7.2	3.3	3.3	5.7
5	4.7	6.8	9.0	4.7	4.7	7.2
6	6.8	6.8	10.8	4.7	6.8	8.6
7	6.8	10	12.6	4.7	6.8	10.0
8	10	10	14.4	6.8	6.8	11.5

Table 3: Input Capacitor Selection

To calculate the capacitance required for alternative parameters, use the following equation.

$$C_{in1} + C_{in2} \geq \frac{P_{NOM}}{\eta_{SWLV} * \pi * F_{AC(MIN)} * (2 * V_{AC(MIN)}^2 - V_{DCBRN}^2)} * \arccos\left(\frac{-V_{DCBRN}}{\sqrt{2} * V_{AC(MIN)}}\right)$$

2.2 Switch Component

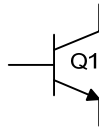


Figure 6: Switch Components

2.2.1 Primary Switch Transistor (Q1)

Selection of the primary switch transistor (Q1) should take in to account the following factors:

- Maximum collector voltage (V_{CE}) it must withstand under all possible operating conditions;
- Maximum collector current (I_C) expected;
- Worst case voltage and current stress it has to withstand during turn off;
- Minimum h_{FE} at peak collector current;
- Turn-off switching characteristics

Table 4 lists example transistor types suitable for use as the primary switch, assuming:

- $V_{CBO} \geq 700$ V
- $V_{CES} \geq 700$ V
- $V_{CEO} \geq 400$ V
- $h_{FE(MIN)} > 8$ @ $V_{CE} = 2$ V when $I_C = I_{C(PK)}$
- $h_{FE(TYP)} > 10$ @ $V_{CE} = 2$ V when $I_C = I_{C(PK)}$

Manufacturers' datasheets should be consulted to ensure that the particular component chosen for Q1 meets the above specifications.

For higher power applications (6 W and above) heat-sinking of the transistor should be considered. A clip-on type rated at $< 80^{\circ}\text{C}\text{W}^{-1}$ is typically adequate. Alternatively, use a larger package like the TO126.

Rated Power P_{NOM} (W)	Example Transistors	
	Type	Package
≤ 3	SBN13001	TO-92
≤ 4	APT13003	TO-92
≤ 8	STX83003	TO-92
	TS13003MV	TO-92
	BUJ100	TO-92
	STBV42	TO-92
	STBV32	TO-92
	STX13003	TO-92
	STX616	TO-92
	ST13003	TO-126

Table 4: Suitable Primary Switch Transistor Types

Maximum ED Pin Voltage

The ED pin voltage needs to be considered during three critical phases of the switching cycle (see Figure 7):

1. The leading edge spike just after Q1 turns off ($V_{EDSPIKE}$);
2. The off state after the leading edge spike (V_{EDOFF});
3. The ringing pulses due to capacitive coupling of collector to emitter while Q1 is off (V_{EDRING})

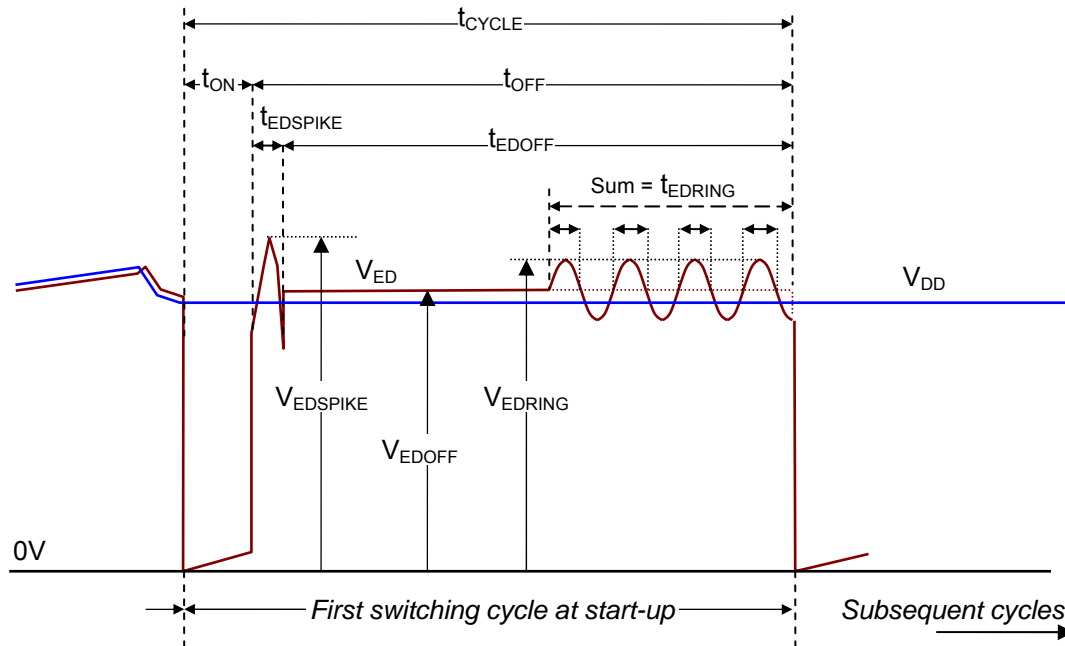


Figure 7: ED and VDD Pin Waveforms

The limits apply under all applicable operating conditions of the product:

- Turn-on, continuous operation and turn-off;
- With any continuous load (including short circuit) or load transition
- For the full range of mains input voltage
- Over the full operating temperature range

For long-term reliability and avoidance of single event destructive failure (e.g. by latch-up or junction breakdown), the following recommendations are given:

1. $V_{EDSPIKE}$ should not exceed $V_{DD} + 1.4\text{ V}$ and should not be above V_{DD} for more than 1% of switching cycle ($t_{EDSPIKE}/t_{CYCLE} \leq 1\%$);
2. The ED pin voltage should not exceed 6.0 V under any circumstances, however short the duration.

Other IC datasheet limits must be obeyed (such as junction temperature no higher than 105°C).

2.3 Transformer Design

Design of the transformer is key for achieving optimum performance. The type, size and construction of the transformer is based on the nominal rated power output, the input voltage, size of the power supply and target cost. Transformer designs described in this document have four functional windings: primary (P), secondary (S), auxiliary (A) and feedback (F).

2.3.1 Core Size Selection

Choice of core size depends on the application requirements for cost, power rating, leakage inductance and EMC performance. Table 5 gives recommended sizes for typical applications based on nominal rated power. The recommendations assume use of low-loss core material suitable for 50 kHz operation, e.g. PC40, and an output voltage of 5 V.

Rated Power P_{NOM} (W)	Recommended Core Size	Winding Topology
1 – 4	E13/6/6	WT2
3 – 5		WT3
5 – 6	E16/8/5	WT4
7-8	E16/8/5	WT5

Table 5: Core Size and Winding Topology Selection

The leakage inductance for all winding topologies should be minimised:

- $L_{L(P/S)} < 100 \mu\text{H}$
- $L_{L(P/A)} < 40 \mu\text{H}$

2.3.2 Transformer Schematics

Figure 8 shows the four different transformer winding topologies described in this design guide. The choice of winding configuration depends on the required output power rating as specified in Table 5.

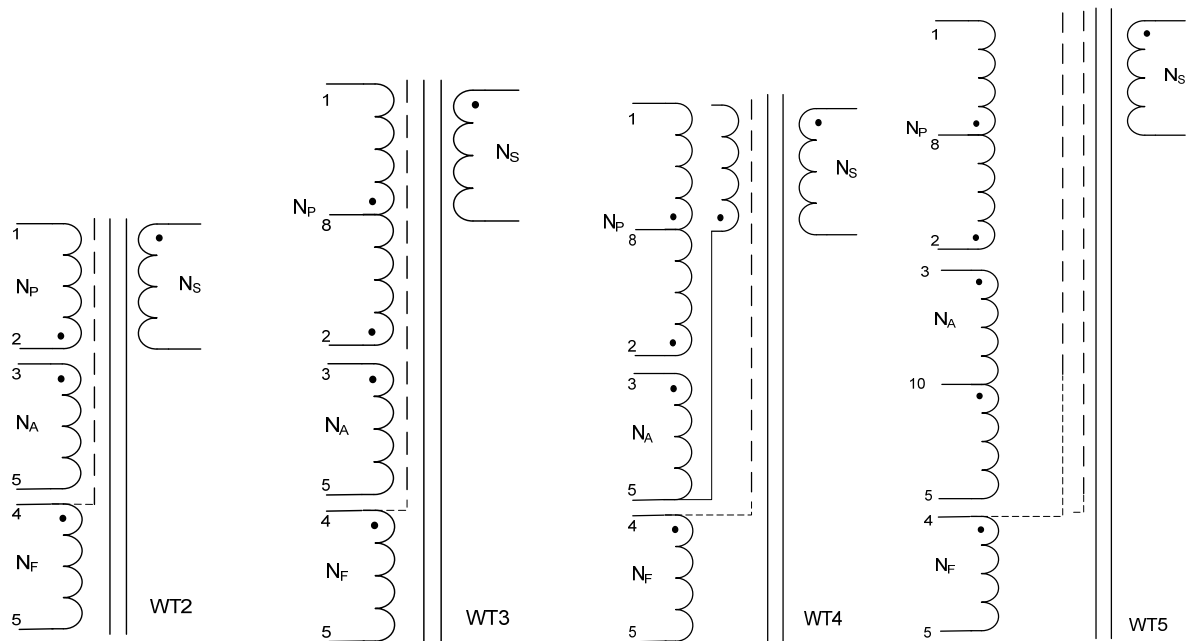


Figure 8: Transformer Schematics for Different Winding Topologies

2.3.3 Number of Primary Turns (N_P)

Based on the required full load system efficiency (η_{NOM}), rated power (P_{NOM}) and nominal switching frequency (F_{NOM}), the nominal primary inductance ($L_{P(NOM)}$) of the transformer can be calculated. The peak primary current can also be calculated based on the required rated power and efficiency. Using these calculated values, the minimum number of primary turns required can be calculated.

The following table assumes a nominal duty cycle (D_{NOM}) of 45% and minimum rectified input voltage ($V_{DC(MIN)}$) of 70 V. The B_{MAX} of the transformer should not exceed 350 mT. The transformer core area (A_E) for an E13 core is assumed as 17.1 mm^2 , and for an E16 core is assumed as 19 mm^2 .

P_{NOM} (W)	η_{NOM} (%)	$I_{P(PK)}$ (mA)	Core Type	A_E (mm ²)	F_{MAX} (kHz)	$L_{P(NOM)}$ (mH)	$N_{P(MIN)}$
1	64.2%	82	E13	17.1	50	9.3	160
2	68.5%	154	E13	17.1	50	4.9	160
3	71.1%	223	E13	17.1	50	3.4	160
4	72.9%	290	E13	17.1	50	2.6	160
5	74.3%	356	E13	17.1	50	2.1	160
6	75.4%	421	E16	19	50	1.8	160
7	76.4%	485	E16	19	50	1.6	160
8	77.2%	548	E16	19	50	1.4	160

Table 6: Primary Inductance and Turns Selection

To calculate for other designs, use the following formulae.

$$L_{P(NOM)} = \frac{V_{DC(MIN)} * D_{NOM}}{I_{P(PK)} * F_{NOM} * 1.05}$$

$$I_{P(PK)} \approx \frac{2 * P_{NOM}}{\eta_{NOM} * V_{DC(MIN)} * D_{NOM}}$$

$$N_{P(MIN)} \approx \frac{L_{P(NOM)} * I_{P(PK)}}{B_{MAX} * A_E}$$

$$A_{L(NOM)} = \frac{L_{P(NOM)}}{N_P^2}$$

Note that reducing the primary inductance has the effect of increasing the operating frequency. It also reduces the peak flux if the turns are not changed.

2.3.4 Number of Secondary Turns (N_S), Auxiliary Turns (N_A) and Feedback Turns (N_F)

Having calculated the number of primary turns required, the other turns ratios can be calculated.

Table 7 assumes the primary turns (N_P) have been chosen to be 160, the cable compensation (G_{CAB}) is 5%, minimum rectified input voltage ($V_{DC(MIN)}$) is 70 V, auxiliary voltage (V_{AUX}) is 4 V and D_{NOM} is 45%.

V_{NOM} (V)	Primary		Secondary		Feedback	
	N_P	N_S	Wire		N_F	Wire
			E13	E16		
4.2	160	6	1 x 0.8 mm	1 x 1. mm	3	1 x 0.10 mm
5	160	8	1 x 0.6 mm	1 x 0.7 mm	4	1 x 0.10 mm
6.5	160	10	1 x 0.5 mm	1 x 0.6 mm	5	1 x 0.10 mm
9	160	14	1 x 0.3 mm	1 x 0.4 mm	7	1 x 0.10 mm
12	160	19	1 x 0.5 mm	1 x 0.7 mm	10	1 x 0.10 mm
15	160	24	1 x 0.4 mm	1 x 0.5 mm	12	1 x 0.10 mm
18	160	28	1 x 0.3 mm	1 x 0.4 mm	14	1 x 0.10 mm
24	160	38	1 x 0.2 mm	1 x 0.2 mm	19	1 x 0.10 mm

Table 7: Secondary, Auxiliary and Feedback Turns Selection

The turns ratios for other designs can be calculated as below. N_S should be truncated values, N_F and N_A should be rounded up.

$$\frac{N_P}{N_S} = \frac{V_{DC(MIN)}}{V_{NOM} * (1 + G_{CAB})} * \frac{D_{MAX}}{(1 - D_{MAX})}$$

$$\frac{N_A}{N_S} = \frac{V_{AUX}}{V_{NOM} * (1 + G_{CAB})}$$

$$\frac{N_S}{N_F} = 2$$

2.3.5 Windings Topologies

In the following tables, the secondary and feedback turns can be determined from Table 7.

For up to 4 W, WT2 includes a feedback winding, allowing the output voltage ripple to be minimised.

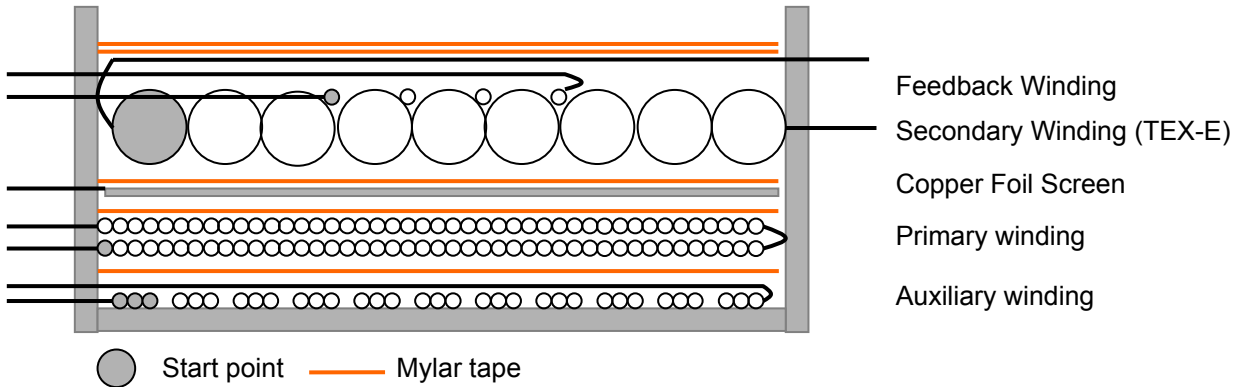


Figure 9: WT2 Transformer Winding Arrangement

WT2 Winding	Type	Wire	Wire Turns	Wire Layers	Tape Turns
W1	Auxiliary	3 x 0.23 mm ECW	7	1	1
W2	Primary	1 x 0.104 mm ECW	160	3	1
W3	Screen	7 x 28 mm Cu foil	1	1	1
W4	Secondary	See Table 7			0
W5	Feedback				2
W6	Flux-band	1 x 0.2 mm TCW	2	1	0

Table 8: WT2 Transformer Winding Configuration

For 3-5 W, WT3 has a split primary that gives lower peak voltages on the Q1 collector, but slightly lower overall system efficiency than WT2.

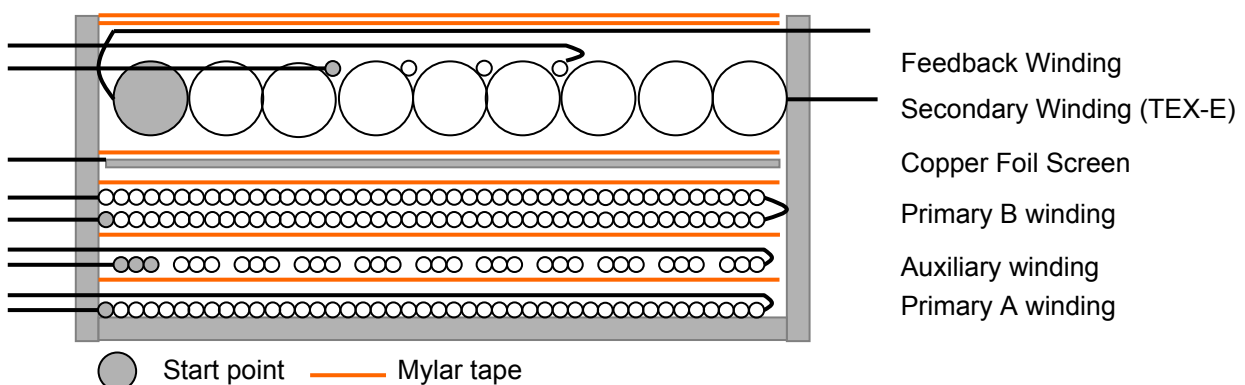


Figure 10: WT3 Transformer Winding Arrangement

WT3 Winding	Type	Wire	Wire Turns	Wire Layers	Tape Turns
W1	Primary A	1 x 0.103 mm ECW	53	1	1
W2	Auxiliary	3 x 0.23 mm ECW	7	1	1
W3	Primary B	1 x 0.103 mm ECW	107	2	1
W4	Screen	7 x 28 mm Cu foil	1	1	1
W5	Secondary	See Table 7			0
W6	Feedback				2
W7	Flux-band	1 x 0.20 mm TCW	2	1	0

Table 9: WT3 Transformer Winding Configuration

For 5-6 W, WT4 has a split primary and screened core that gives lower peak voltages on the Q1 collector, but slightly lowers overall system efficiency. The start of the screen winding is connected to a DC level such as the rectified line.

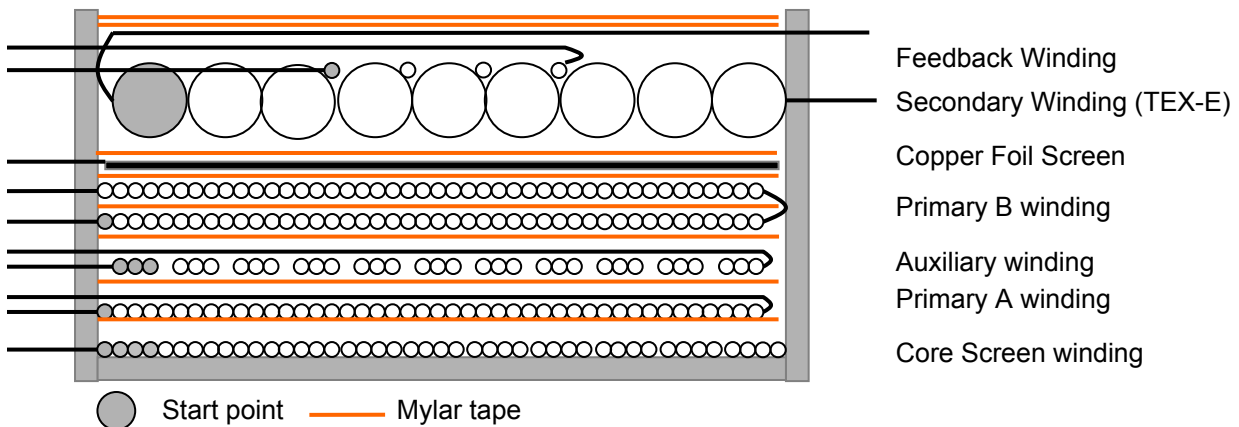


Figure 11: WT4 Transformer Winding Arrangement

WT4 Winding	Type	Wire	Wire Turns	Wire Layers	Tape Turns
W1	Core Screen	2 x 0.15 mm ECW	24	1	1
W2	Primary A	1 x 0.14 mm ECW	53	1	1
W3	Auxiliary	3 x 0.32 mm ECW	7	1	1
W4	Primary B	1 x 0.14 mm ECW	107	2	1
W5	Screen	7 x 28 mm Cu foil	1	1	1
W6	Secondary	See Table 7			0
W7	Feedback				2
W8	Flux-band	1 x 0.20 mm TCW	2	1	0

Table 10: WT4 Transformer Winding Configuration

For 6-8 W, WT5 has a split primary around the secondary that reduces losses due to leakage inductance effects. Note that the secondary winding is best kept to a single layer for EMC performance.

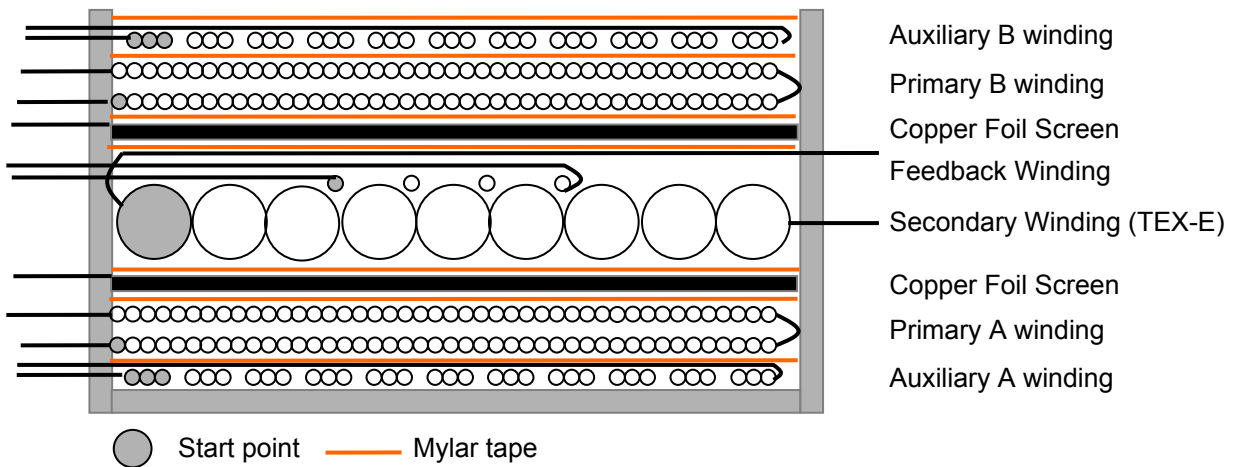


Figure 12: WT5 Transformer Winding Arrangement

WT5 Winding	Type	Wire	Wire Turns	Wire Layers	Tape Turns
W1	Auxiliary A	3 x 0.32 mm ECW	4.0	1	1
W2	Primary A	1 x 0.14 mm ECW	80	2	1
W3	Screen	7 x 28 mm Cu foil	1	1	1
W4	Secondary	See Table 7			0
W5	Feedback				1
W6	Screen	7 x 28 mm Cu foil	1	1	1
W7	Primary B	1 x 0.14 mm ECW	80	2	1
W8	Auxiliary B	3 x 0.32 mm ECW	3.0	1	1
W9	Flux-band	1 x 0.20 mm TCW	2	1	0

Table 11: WT5 Transformer Winding Configuration

2.4 Controller Components

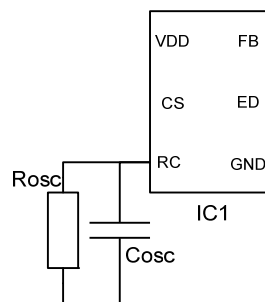


Figure 13: Controller Components

2.4.1 Controller IC (IC1)

The controller part depends on the nominal output power as shown in Table 12.

P _{NOM} (W)	IC1
Up to 4	C2161PX2
Up to 8	C2162PX2

Table 12: Controller IC Selection

2.4.2 Oscillator Resistor and Capacitor (R_{osc} and C_{osc})

The oscillator components determine the maximum controller switching frequency (F_{NOM}) and the cable compensation (G_{CAB}). (Note: the minimum frequency limit is set by the auxiliary and VDD components, see section 2.7).

2.4.2.1 Cable Compensation

Cable compensation requirements depend on the cable, output voltage and output current as shown in Table 13. This assumes a cable length of 1.8 m and a minimum C_{osc} of 220 pF. If the cable compensation requires a capacitor value for C_{osc} of less than 220 pF, no value is given.

V _{NOM} (V)	I _{NOM} (A)	G _{CAB} (x100%)				C _{osc} (pF)			
		22 AWG	24 AWG	26 AWG	28 AWG	22 AWG	24 AWG	26 AWG	28 AWG
5	0.2			1.6	2.8			1200	750
5	0.4		1.7	3.2	5.5		1200	620	360
5	0.6	1.2	2.6	4.8	8.3	1800	750	430	240
5	0.8	1.6	3.4	6.4		1300	560	330	
5	1.0	1.9	4.3	8.0		1000	470	270	
5	1.2	2.3	5.1	9.6		820	390	220	
5	1.4	2.7	6.0			750	330		
5	1.6	3.1	6.8			620	300		

Table 13: Oscillator Capacitor Selection

The cable compensation (G_{CAB}) and oscillator capacitor (C_{osc}) value can be calculated using the following equations, where K_{CAB} is specified in the IC datasheet (reference DS-2918). R_{FD} is an error term caused by the temperature of the output diode changing in sympathy with the output current. Note that the figures for G_{CAB} in Table 13 have been multiplied by 100%; values used in the equations should not be multiplied.

$$G_{CAB} = \frac{(R_{CABLE} - R_{FD}) * I_{NOM}}{V_{NOM}} \quad R_{FD} = 0.1 \quad C_{osc} = \frac{K_{CAB}}{G_{CAB}}$$

2.4.2.2 Switching Frequency

The switching frequency is determined by the applied load, as shown in Figure 14. Note: the minimum frequency limit is set by the auxiliary and VDD components, see section 2.7.

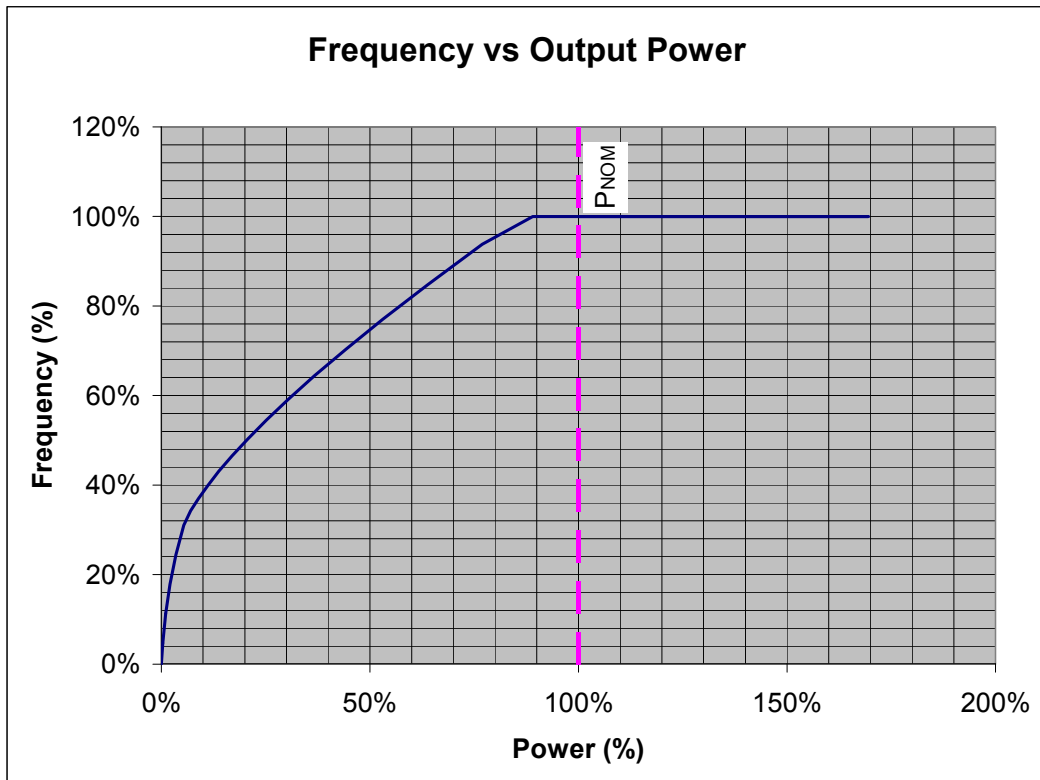


Figure 14: Graph of Switching Frequency vs Load

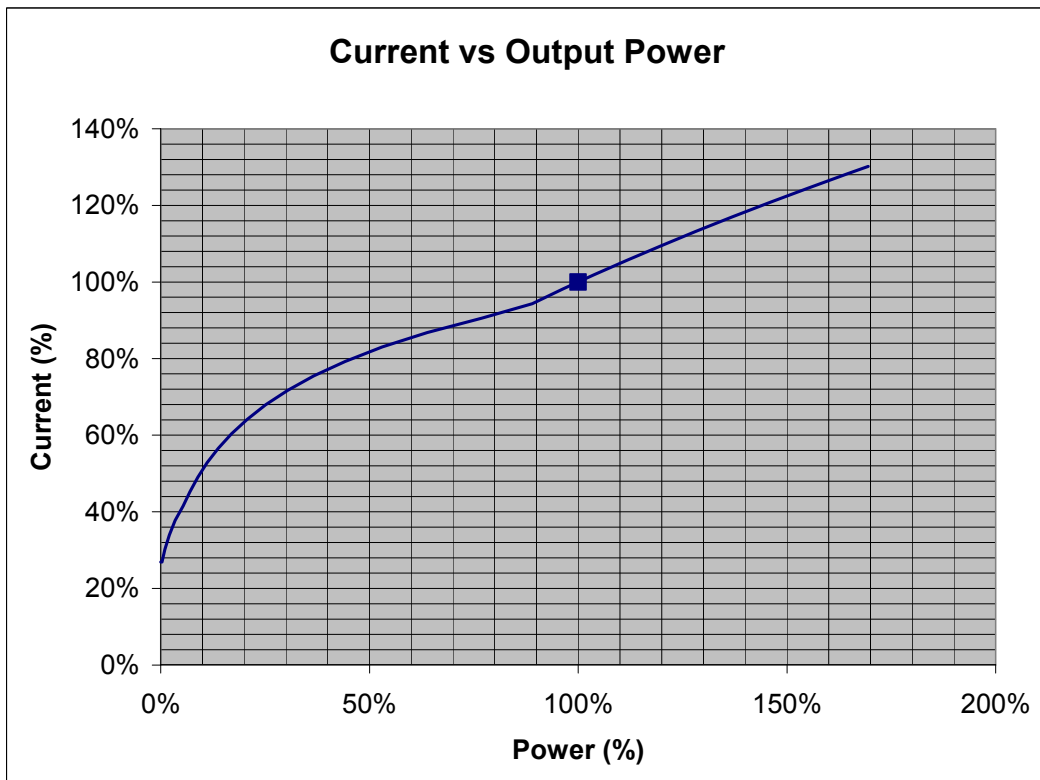


Figure 15: Graph of Peak Primary Current vs Output Power

Based on the required maximum switching frequency, F_{NOM} the oscillator resistor (R_{osc}) value can be determined from Figure 16.

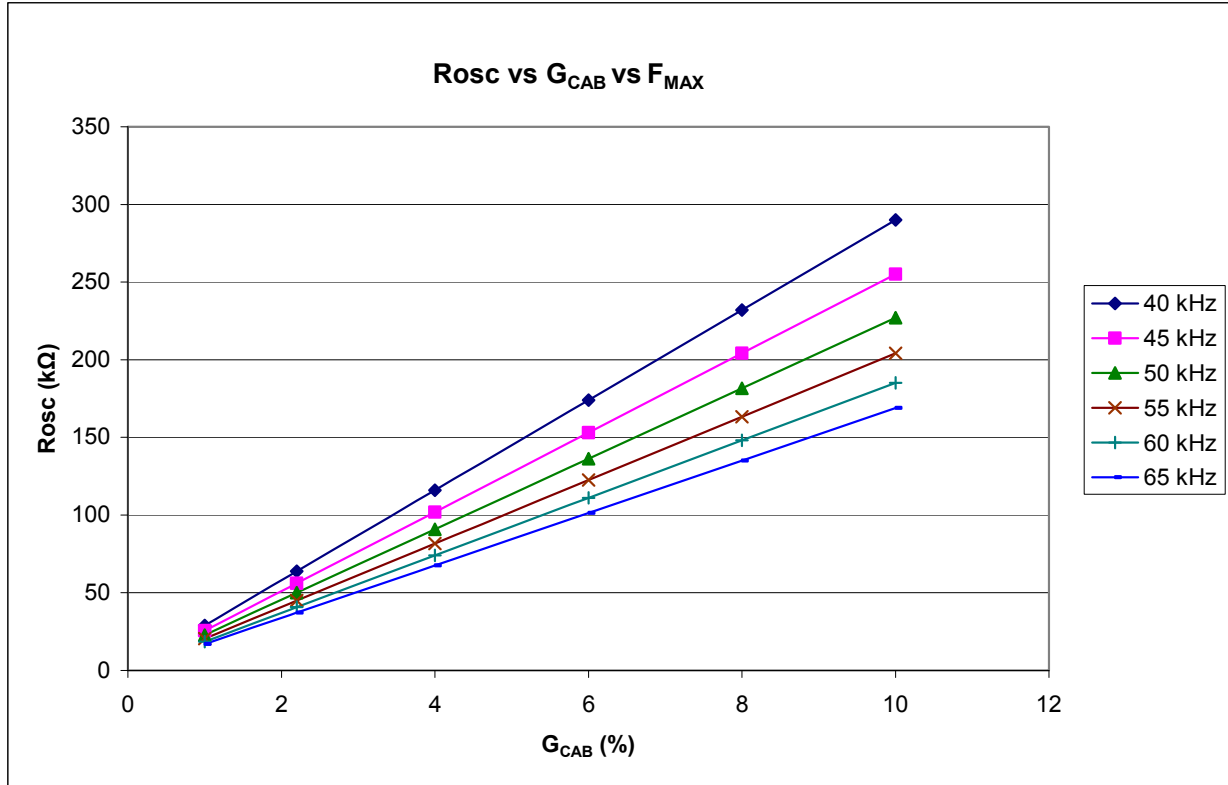


Figure 16: Oscillator Frequency and Resistor Selection

Alternatively, the value of R_{osc} can be calculated from the following formula. The required oscillation time-constant (T_{osc}) needs to be calculated, before the R_{osc} can be calculated. K_{osc} and t_{RCRST} are specified in the IC datasheet (reference DS-2918).

$$T_{osc} = \frac{(1/F_{NOM}) - t_{RCRST}}{K_{OSC}}$$

$$R_{osc} = \frac{T_{osc}}{C_{osc}}$$

2.5 Feedback Components

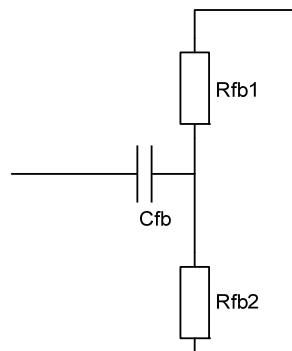


Figure 17: Feedback Components

2.5.1 Feedback Resistors (Rfb1 and Rfb2)

The voltage sensing feedback resistors scale the transformer auxiliary winding waveform to match the controller IC feedback (FB) input.

V _{NOM} (V)	Primary	Secondary	Auxiliary	Feedback	WT2-5			V _{DF} (V)
	N _P	N _S	N _A	N _F	Rfb1/ Rfb2 (Ω)	Rfb1 (Ω)	Rfb2 (Ω)	
4.2	160	6	7	3	4.42	1300	300	0.25
5	160	8	7	4	5.40	1100	200	0.25
6.5	160	10	7	5	7.23	1300	180	0.25
9	160	14	7	7	10.27	1200	120	0.25
12	160	19	7	10	15.23	3000	200	0.65
15	160	24	7	12	18.07	4000	220	0.65
18	160	28	7	14	21.73	3300	150	0.65
24	160	38	7	19	29.04	3200	110	0.65

Table 14: Feedback Resistor Selection

To calculate values for other designs, use the following formulae. ΔV_{FBREG} and $\Delta V_{FB}/\Delta t$ are specified in the IC datasheet (ref DS-2918). F_{RES} is the transformer resonance frequency (in-circuit), 400 kHz in this case. t_{FB} is the feedback adjustment factor, 70 ns. V_{DF} is the forward conduction voltage of output diode D_{out} . The Rfb1 and Rfb2 combination should be chosen from standard resistor values to give the best match to the desired ratio Rfb1/Rfb2, while ensuring the parallel value is less than 300 Ω.

$$V_{FBX} = \sqrt{\Delta V_{FBREG}^2 + \left(\frac{\Delta V_{FB}}{\Delta t} * \left(\frac{1}{2 * \pi * F_{RES}} - t_{FB} \right) \right)^2} \quad \frac{Rfb1 * Rfb2}{Rfb1 + Rfb2} \leq 300\Omega$$

$$\frac{Rfb1}{Rfb2} = \frac{(V_{NOM} + V_{DF}) * N_F - 1}{V_{FBX} * N_S}$$

2.5.2 FB Coupling Capacitor (Cfb)

The FB coupling capacitor selection is 47 nF Y5V/25V.

2.6 Current Sense Components

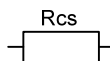


Figure 18: Current Sense Component

2.6.1 Current Sense Resistor (Rcs)

The output current limit is set by the current sense resistor. Figure 19 allows the value of the Rcs to be selected according to the output power requirements. NB Rounding ideal values up will result in a lower constant current value; rounding down will give a higher constant current.

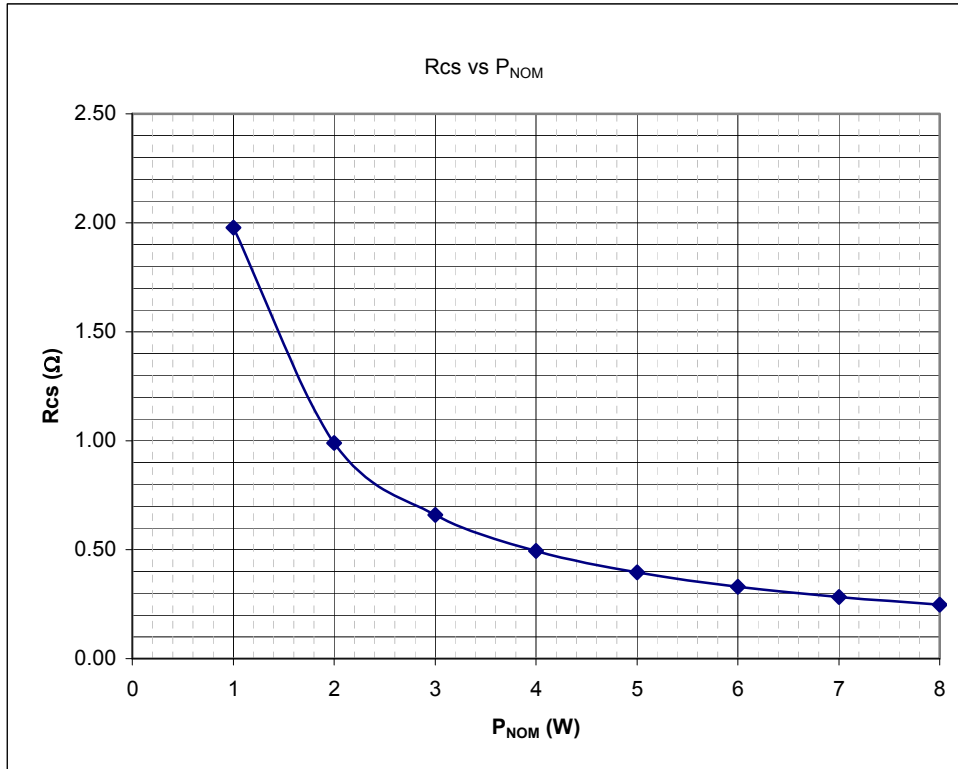


Figure 19: Current Sense Resistor Selection Based on Nominal Power

Alternatively use the following formula, where $V_{CS\text{CC}}$ is specified in the IC datasheet (reference DS-2918) and η_{SWLV} is assumed as 90%.

$$R_{CS} = \frac{N_P}{N_S} * \frac{V_{CS\text{CC}} * \eta_{\text{SWLV}}}{I_{\text{REG}}}$$

2.7 VDD and Auxiliary Components

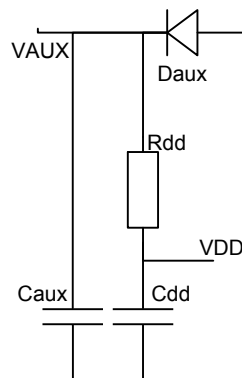


Figure 20: VDD and Auxiliary Components

When designing the PCB, ensure that the loop formed by Caux, Daux and T1 is as short as possible.

2.7.1 Auxiliary Supply Capacitor (Caux)

The auxiliary supply capacitor is used, together with the Cdd capacitor, as a timing component, defining the minimum switching frequency (at no-load). For the basis of this design guide, a switching frequency of 1.5 kHz will be the target. NB It is dependant on whether a secondary or primary snubber is used. The following graph assumes no snubbers are used, but will provide a good starting point value for Caux for all designs.

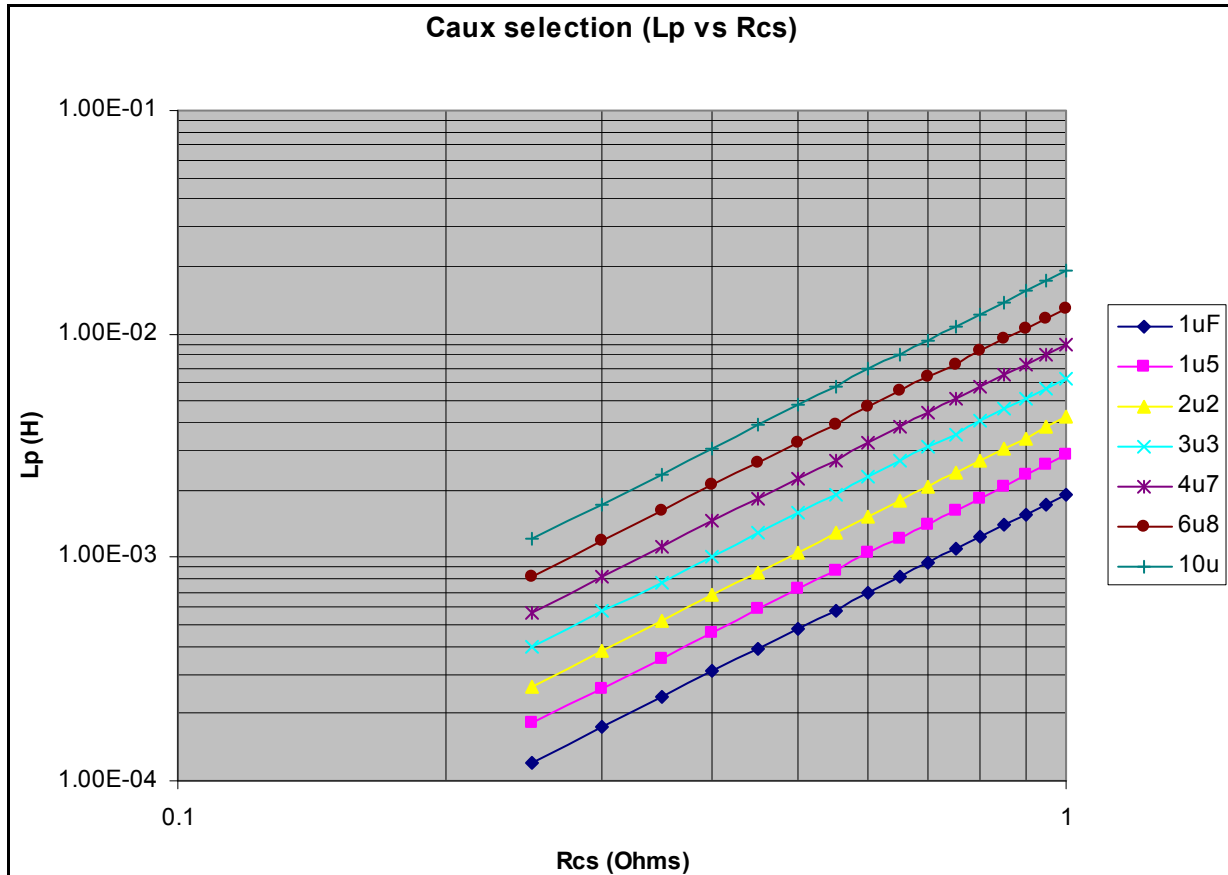


Figure 21: Caux Selection

This comes from the equation:

$$C_{aux} = \frac{1.3 * \left[L_p \left(\frac{V_{CSMIN}}{R_{cs}} \right)^2 - C_{psnub} \left(V_{NOM} \cdot \frac{N_P}{N_S} \right)^2 - C_{ssnub} * (V_{NOM})^2 \right]}{(V_{AUXHI}^2 - V_{AUXLO}^2)}$$

Where $V_{AUXLO} = V_{DDREG} - \Delta V_{DDSLEEP} / 3$ and $V_{AUXHI} = V_{NOM} \cdot \frac{N_A}{N_S} - V_{DAUX}$

And V_{CSMIN} , V_{DDREG} and $\Delta V_{DDSLEEP}$ are specified in the IC datasheet (reference DS-2918). L_p , R_{cs} , R_{out} , C_{psnub} , C_{ssnub} , N_P , N_S , N_A are defined elsewhere in this document. V_{DAUX} is assumed to be 0.8 V. V_{NOM} is defined by the used.

It may be necessary to use two capacitors in parallel to achieve the required value. A close tolerance (10%) and good quality dielectric types (X5R or X7R) is required.

No-load Switching Frequency

To avoid potential no-load instability, it is important that the energy delivered from the transformer in each pulse should be sufficient to turn on each diode that is directly connected to the transformer. This places a lower limit on the transformer energy. To avoid output voltage rising under no-load conditions, the total transformer energy must be less than the energy required to top up all the attached capacitances. These two conditions place upper and lower limits on the transformer energy. With these constraints, the target value of F_{MIN} should be between 1 kHz and 2 kHz. C_{aux} should be adjusted to ensure this is achieved.

2.7.2 Auxiliary Supply Diode (Daux)

The auxiliary diode is used to capture the short pulse of energy that is related to the leakage inductance of the transformer, and therefore needs to have high peak current handling and fast recovery times. For this reason, Daux is selected to have the following preferred parameters:

- $T_{RR} < 50\text{ns}$ (reverse recovery time)
- $V_{RRM} > 40\text{V}$ (repetitive peak reverse voltage)
- $V_{FD} < 1\text{V} @ I_F = I_{AUXF}$ (forward voltage @ forward current, under no-load condition), where

$$I_{AUXF} \approx 2 * I_{DDREG} \left(\frac{V_{CS(MAX)}}{V_{CS(MIN)}} \right) \left(\frac{F_{NOM}}{F_{MIN}} \right) \left(\frac{1}{D_{NOM}} \right)$$

A selection of suitable diodes is given below in Table 15. Selecting a diode with larger (inferior) V_{FD} may result in output voltage lifting under no-load conditions.

Type	T_{RR} (ns)	V_{RRM} (V)	V_{FD} (V) @	I_F (A)
1N4148	4	75	1.0	0.15
1N4933	50	50	1.0	1.0
SF11G	35	50	1.0	2.0
UF4001	50	50	1.0	2.0
BYV27-50	25	50	1.0	2.0
UG1A	25	50	1.0	3.0
ES1A	35	50	1.0	3.0
STTH1R02	15	200	1.0	3.0

Table 15: Daux Selection - Suitable Diode Types

2.7.3 VDD Capacitor (Cdd)

The VDD capacitor selection is 2.2 μF 10% 10V (X5R or X7R). It is important that the value of Cdd is not greater than 4 μF . The VDD capacitor is used, together with the C_{aux} capacitor, as a timing component controlling the switching frequency at no-load. It is therefore important that the tolerance ($\pm 10\%$) and dielectric (X5R or X7R) are correctly chosen.

PCB tracks from the controller to Cdd should be as short as possible, and no more than 5 mm. Longer tracks can cause poor circuit performance.

2.7.4 VDD Resistor (Rdd)

The VDD feed resistor must provide sufficient supply current to IC1 via the VDD pin, at minimum auxiliary winding voltage (about 4 V) during no-load, but must dissipate minimum power to limit no-load power. The value of Rdd is typically in the range 200 to 500 Ω , and is given by the following equation:

$$R_{dd} = \left(\frac{V_{AUX} - V_{DDMIN}}{I_{DDREG}} \right) \left(\frac{C_{dd} + C_{aux}}{C_{aux}} \right)$$

2.8 Output Components

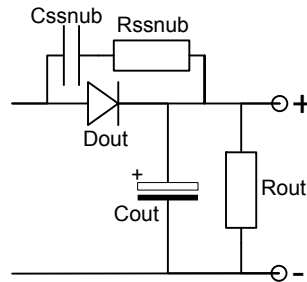


Figure 22: Output Components

2.8.1 Output Diode (Dout)

The output diode must withstand continuous operation under overload conditions and reverse voltage at peak input voltage. For efficiency reasons, Schottky diodes are better for output voltages (V_{NOM}) up to 12 V. Above 12 V, fast epitaxial diodes are more suitable.

In Table 16, the minimum recommended reverse voltage rating (V_{RRM}) and the minimum recommended average forward current handling capability ($I_{F(AV)}$) for example diodes are given. Based on these, the maximum nominal voltage and current can be determined, assuming a maximum input mains voltage ($V_{AC(MAX)}$) of 265 Vac and cable compensation (G_{CAB}) of 5%. This also assumes de-rating factors of 50% for forward average current $I_{F(AV)}$ and 25% de-rating for reverse voltage V_{RRM} . Choose a higher $I_{F(AV)}$ for increased efficiency.

Example Diode Selections			Maximum Values	
Type	$I_{F(AV)}$ (A)	V_{RRM} (V)	V_{NOM} (V)	I_{NOM} (A)
SB140	1	40	5.1	0.5
21DQ04	2	40	5.1	1
SB340	3	40	5.1	1.5
SB540	5	40	5.1	2.5
SB160	1	60	7.6	0.5
STPS2L60	2	60	7.6	1
STPS3L60	3	60	7.6	1.5
50SQ080	5	80	10.1	2.5
1N4934	1	100	12.7	0.5
HER152	1.5	100	12.7	0.75

Table 16: Output Diode Selection

To calculate the minimum recommended reverse voltage rating, use the following formula. This includes the 25% de-rating factor.

$$V_{RRM} = [V_{NOM} * (1 + G_{CAB}) + (\sqrt{2} * V_{AC(MAX)} * \frac{N_s}{N_p})] / 0.75$$

To calculate the minimum recommended average forward current handling capability:

$$I_{F(AV)} = 0.5 * I_{CCMIN} * (1 + 0.5 * K_{CCTOL})$$

A heat sink may be required on Dout in higher power applications.

2.8.2 Output Capacitor (Cout)

The output capacitor is selected according to ripple current rating, effective series resistance (ESR), operating temperature, lifetime, size and cost requirements. In the application, the output capacitor(s) are required to have a lifetime of 3650 hours minimum (1 hr/day for 10 years) at 85°C. NB The capacitor lifetime and ripple current data is given at 105°C.

Table 17 shows example output capacitor values based on nominal current. It may be necessary to have two or more capacitors in parallel. The ripple current rating is also given. The maximum duty cycle (D_{MAX}) is assumed as 50% and the transformer inductance tolerance (K_{LPTOL}) as 10%.

I_{NOM} (A)	I_{RIPPLE} (mA) (actual)	Cap Type 500mA*		Cap Type 750mA*		Cap Type 1000mA*	
		Qty	uF	Qty	uF	Qty	uF
0.2	280	1	100	1	100	1	100
0.4	560	1	220	1	220	1	220
0.6	840	2	150	1	330	1	330
0.8	1,120	2	220	2	220	1	470
1.0	1,400	3	150	2	330	2	330
1.2	1,680	3	220	2	330	2	330
1.4	1,960	4	220	3	220	2	330
1.6	2,240	4	220	3	330	2	470

Table 17: Output Capacitor Selection

* Manufacturers' current rating assumes 2000 hours life at 105°C

To calculate the current ripple, use the following formula. If it is necessary to increase ripple current rating of capacitors, it is better to increase voltage rating and can size, rather than increase capacitance.

$$I_{RIPPLE} = I_{NOM} * \sqrt{\frac{4}{3 * (1 - D_{MAX} * (1 + K_{LPTOL}))}} - 1$$

The recommended minimum DC voltage rating for C_{out} is $V_{DC} \geq V_{NOM}$. The recommended output capacitance is approximately given by the following equations:

$$C_{out_{(nom)}} \approx \frac{100 * I_{CCMIN}}{V_{NOM} * F_{NOM} * (1 - 0.5 * K_{CCTOL})} \mu F$$

$$C_{out_{(min)}} \approx 0.3 * C_{out_{(nom)}} \mu F$$

$$C_{out_{(max)}} \approx 3 * C_{out_{(nom)}} \mu F$$

If a particular application has to accommodate output capacitance $> C_{out_{(max)}}$, additional measures may be required to maintain loop stability.

2.8.3 Output Resistor (Rout)

The output resistor is required to hold the output voltage down under no-load conditions. The value of Rout is chosen to dissipate the same power as the auxiliary rail (8 mW) which is necessary to maintain good stability under no-load conditions.

Figure 23 gives example Rout values for snubberless applications a range of nominal output voltages.

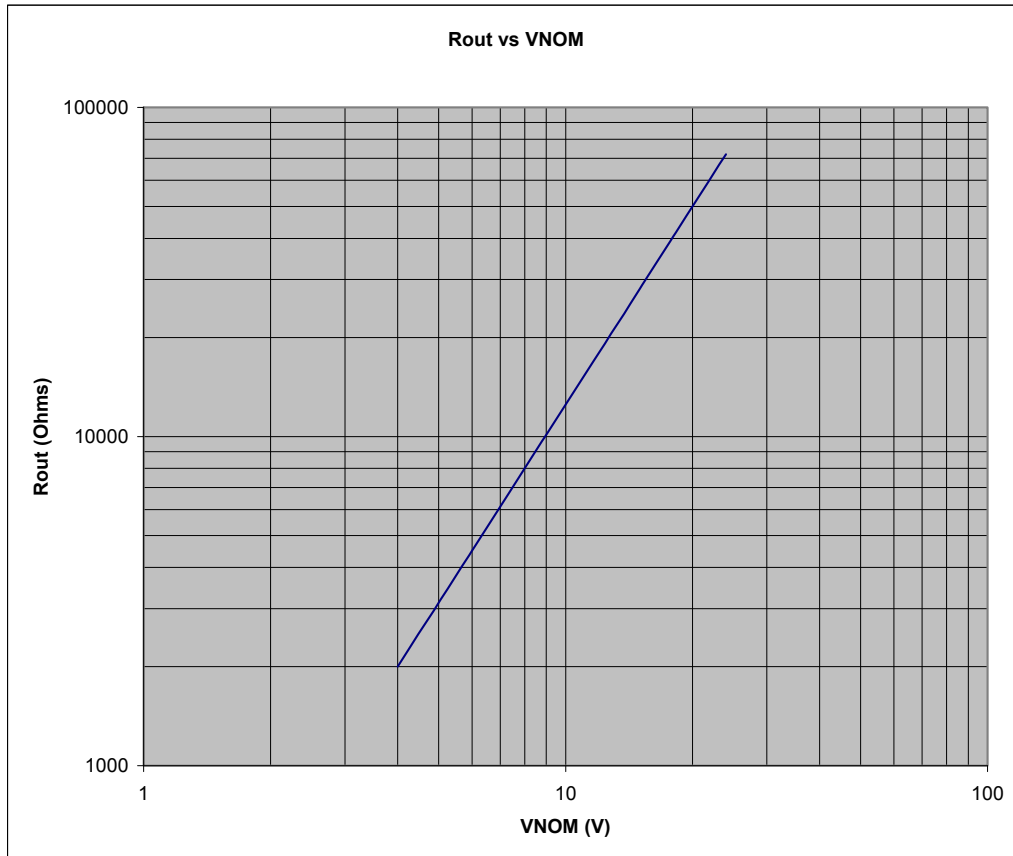


Figure 23: Output Resistor Selection

The equation for Rout is given below.

$$R_{out} = V_{NOM}^2 / P_{DUMMY}$$

2.8.4 Secondary Snubber Resistor and Capacitor (R_{snub} and C_{snub})

A secondary snubber is recommended for applications with $P_{NOM} \geq 3\text{ W}$, to achieve EMC compliance. The optimum values for R_{snub} and C_{snub} are found by experimentation. Increase the value of C_{snub} to improve EMC margin. Decrease C_{snub} to improve margin on no-load power, efficiency and input over-voltage protection.

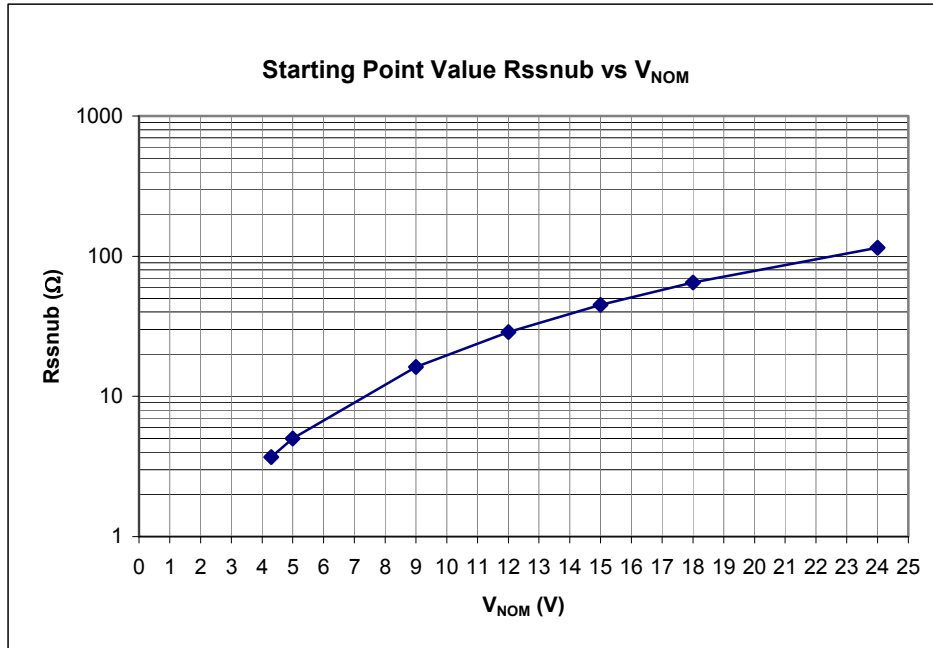


Figure 24: Starting Point Value for Secondary Snubber Resistor

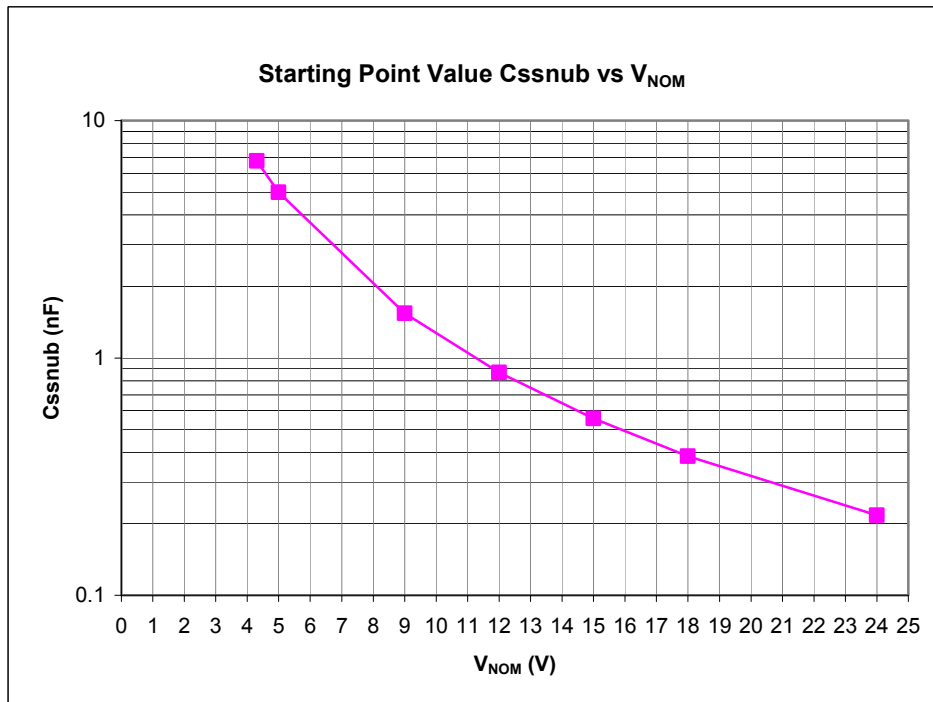


Figure 25: Starting Point Value for Secondary Snubber Capacitor

The starting point values for R_{ssnub} and C_{ssnub} are given by the equations:

$$R_{ssnub} = \frac{V_{NOM}^2}{5} \qquad C_{ssnub} = \frac{125}{V_{NOM}^2} \text{ nF}$$

Note that adding a secondary snubber will affect the calculated value for C_{aux} in section 2.7.1.

2.9 Minimising the Bill of Materials

2.9.1 Minimal Input Filter

To reduce BOM count, it is possible to use the following input configuration. While this configuration saves on component count, achieving EMC compliance is harder and places more constraints upon the choice of L_{filt} and C_{in1} . It is therefore not recommended for applications with $P_{NOM} > 3 \text{ W}$.

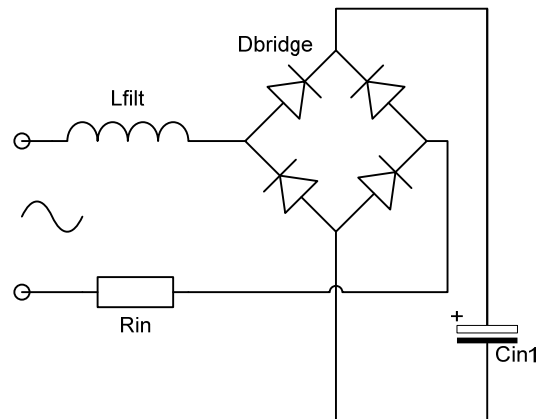


Figure 26: Input Rectifier and Filter Components

For the same conditions as given in 2.1.4, the resulting C_{in1} value would be greater than the minimum total calculated in Table 3. In this case, the C_{in1} capacitance is calculated by:

$$C_{in1} \geq \frac{P_{NOM}}{\eta_{SWLV} * \pi * F_{AC(MIN)} * (2 * V_{AC(MIN)}^2 - V_{DCBRN}^2)} * \arccos\left(\frac{-V_{DCBRN}}{\sqrt{2} * V_{AC(MIN)}}\right)$$

The input inductor moves position. In this configuration, the peak currents through the inductor are higher than in the basic configuration. Therefore, the inductor should be chosen to avoid saturation at peak currents. It is also harder to achieve low conducted emissions in the region 150 kHz to 1 MHz, due to differential-mode currents flowing through C_{in1} , which requires C_{in1} to be chosen for low ESR qualities and L_{filt} to be chosen for non-saturation and self-resonant frequency above 1 MHz. A starting value of 2.2 mH can be selected.

The same bridge rectifier and inrush limiter resistor are used.

2.9.2 Secondary Snubber Elimination

It is possible to remove the secondary-side snubber components C_{ssnub} and R_{ssnub} for applications with $P_{NOM} \leq 3 \text{ W}$.

3 NORMAL BOOTSTRAP OPTION

The normal bootstrap option is suitable for low power ($P_{NOM} < 4\text{ W}$) applications that require no-load power to be $< 150\text{ mW}$. The normal bootstrap option schematic is shown below. The highlighted components are covered by this section.

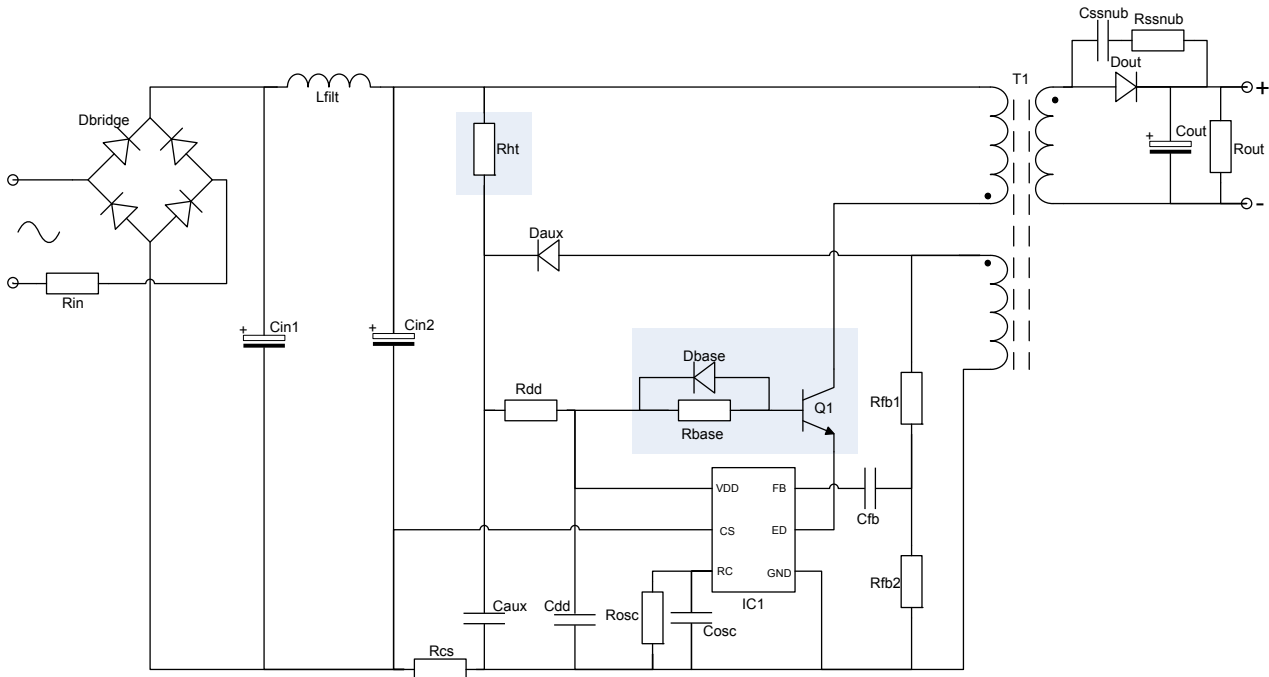


Figure 27: Normal Bootstrap Option Application Schematic

Block	Components	Type / Value	Function
Switch	Dbase	See section 3.1	Switch control components
	Rbase	See section 3.3	
VDD	Rht	See section 3.2	Initial start-up

Table 18: Normal Bootstrap Application Circuit Components

3.1 Base Diode (Dbase)

For applications $< 4\text{ W}$, a 1N4148 is adequate. For applications $> 4\text{ W}$, the designer should consider higher current diodes such as the 1N4933, FR101 or SF11.

3.2 Start-up Resistors (Rht, or Rht1 and Rht2)

The maximum value for the start-up resistor values is $Rht1 + Rht2 = 10\text{ M}\Omega$. There is a trade-off between start-up time and no-load power, dependent on the start-up resistor value; decrease the resistor value to decrease start-up time, but this will also increase no-load power eg $Rht1 = Rht2 = 2.2\text{ M}\Omega$. The resistor(s) combined voltage rating must be able to handle the full input voltage range.

To reduce the BOM count, it is possible to use a single resistor with a higher voltage rating.

3.3 Base Resistor (Rbase)

The base resistor depends on $I_{C(PK)}$ and $h_{FE(TYP)}$. The value is not critical so choose the nearest E12 value. Figure 28 assumes a maximum duty cycle (D_{MAX}) of 50%, a minimum input voltage ($V_{DC(MIN)}$) of 70 V and K_{LPTOL} of 10%. h_{FE} values are estimated from transistor datasheets.

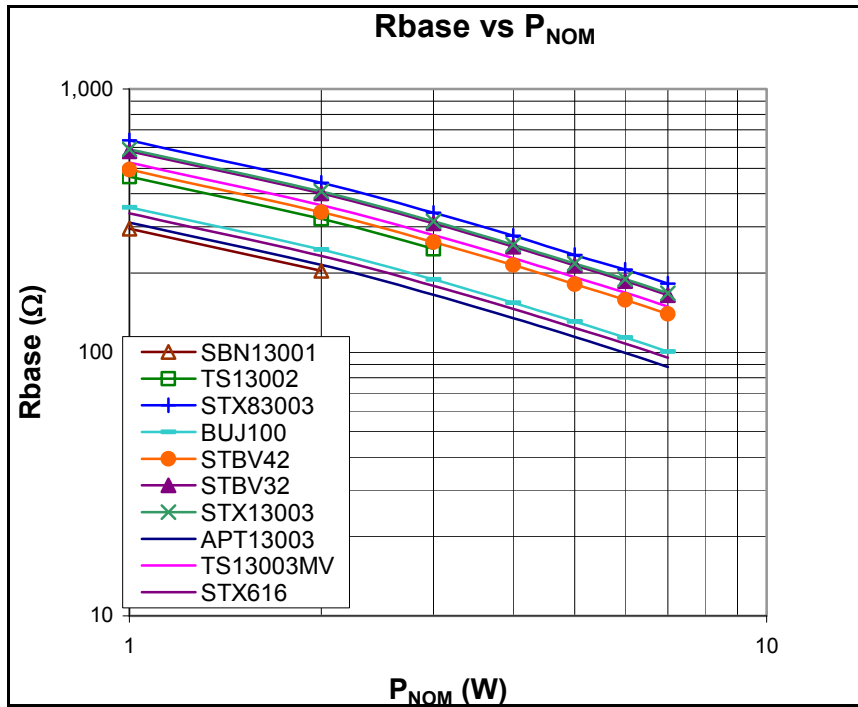


Figure 28: Base Resistor Selection Based on Nominal Power and Transistor Types

For alternative parameter values, calculate the peak collector current using the following equation.

$$I_{C(PK)} = \frac{2 * P_{NOM}}{\eta_{NOM} * V_{DC(MIN)} * D_{NOM}} \quad D_{NOM} = D_{MAX} * (1 - K_{LPTOL})$$

The base resistor value can then be calculated using the following equation.

$$R_{base} = \frac{(V_{DD} - V_{BE(Q1)}) * h_{FE(TYP)}}{I_{C(PK)}}$$

Ideally, the user should find the h_{FE} value for the chosen transistor measured at the peak collector current and saturation voltage of 2 V from the manufacturer's datasheet. However, datasheets do not always have this level of detail and this data may need to be estimated or interpolated from the given data.

4 SUPER BOOTSTRAP OPTION

The super bootstrap option allows the no-load power to be reduced compared to the basic configuration. This option is also required for higher power applications ($P_{NOM} > 4\text{ W}$), in order to isolate the VDD pin from noise caused by Q1 high switching currents. The super bootstrap option schematic is shown below. The highlighted components are covered by this section.

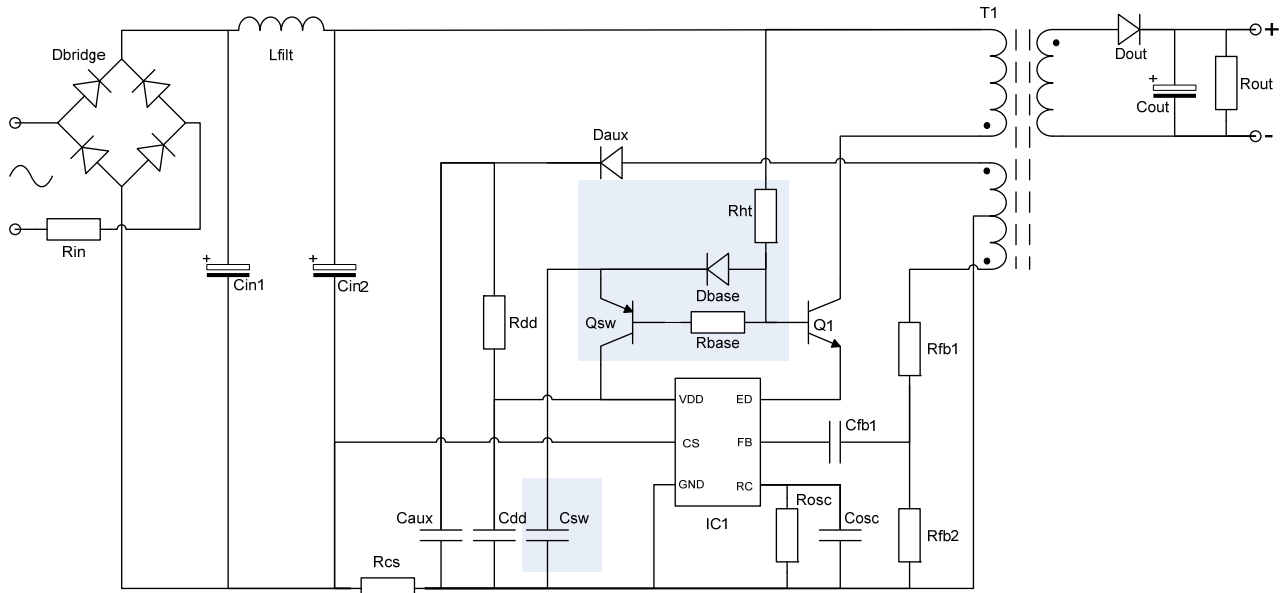


Figure 29: Super Bootstrap Option Application Schematic

Block	Components	Type / Value	Function
Switch	Qsw	See section 4.1.1	Switch control components
	Csw	See section 4.1.2	
	Dbase	See section 4.1.3	
	Rbase	See section 4.1.5	
VDD	Rht	See section 4.1.4	Initial start-up

Table 19: Super Bootstrap Application Circuit Components

4.1.1 Base Drive Regulator Transistor (Qsw)

The base drive regulator transistor may be any low-cost PNP transistor. The BCX17 is recommended.

4.1.2 Switching Capacitor (Csw)

470 nF is recommended for applications $< 4\text{ W}$, 1 μF for applications $> 4\text{ W}$. The maximum value for Csw can be determined by the equation: $C_{sw} + C_{dd} < 4\ \mu\text{F}$.

4.1.3 Base Diode (Dbase)

For most applications, a 1N4148 is adequate. For designs $> 4\text{ W}$, the designer should consider higher current diodes such as the 1N4933 or SF11.

4.1.4 Start-Up Resistors (Rht, or Rht1 and Rht2)

The permitted value range for the start-up resistor values is $R_{ht1} + R_{ht2} = 10\text{ to }100\ \text{M}\Omega$. There is a trade-off between start-up time and no-load power, dependent on the start-up resistor value; decrease the resistor

value to decrease start-up time, but this will also increase no-load power. The resistor(s) combined voltage rating must be able to handle the full input voltage range.

To reduce the BOM count, it is possible to use a single resistor R_{ht} with a higher voltage rating.

4.1.5 Base Resistor (R_{base})

The base resistor is different from the value used in the standard configuration and is given by the following equations and graph. The value is not critical so choose the nearest E12 value. Figure 30 assumes a maximum duty cycle (D_{MAX}) of 50%, a minimum input voltage ($V_{DC(MIN)}$) of 70 V and K_{LPTOL} of 10%. h_{FE} values are estimated from transistor datasheets.

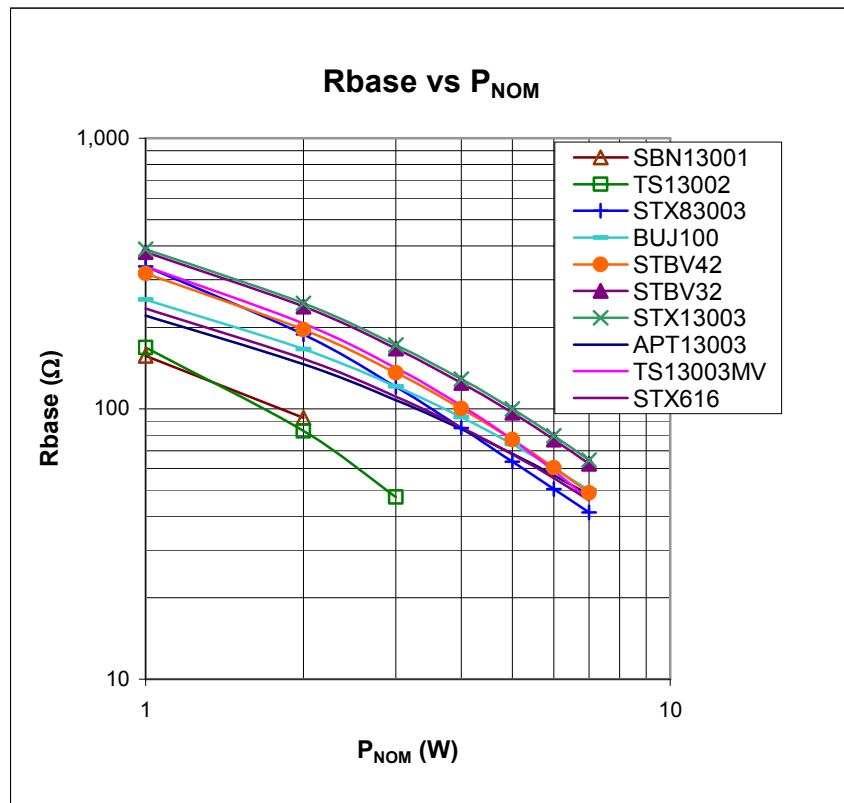


Figure 30: Base Resistor Selection Based on Nominal Power and Transistor Types

For alternative parameter values, calculate the peak collector current using the following equation.

$$I_{C(PK)} = \frac{2 * P_{NOM}}{(\eta_{NOM} * V_{DC(MIN)} * D_{NOM})} \quad D_{NOM} = D_{MAX} * (1 - K_{LPTOL})$$

The base resistor value can then be calculated using the following equation.

$$R_{base} = \frac{(V_{DD} - V_{BE(Q2)} - V_{BE(Q1)}) * h_{FE(TYP)}}{I_{C(PK)}}$$

Ideally, the user should find the h_{FE} value for the chosen transistor measured at the peak collector current and saturation voltage of 2 V from the manufacturer's datasheet. However, datasheets do not always have this level of detail and this data may need to be estimated or interpolated from the given data.

5 ENHANCEMENTS

5.1 Alternative Rcs Arrangement (Rcso1, Rcso2, Rcso3)

Some manufacturers prefer to standardise on a value for $R_{cs} = 1 \Omega$ to minimise BOM cost. In this case, it is necessary to add resistors R_{cso2} and R_{cso3} in order to scale the voltage seen on the CS pin as shown in Figure 31. The following graphs give values for these components. The values can be rounded to the nearest E24 resistor value.

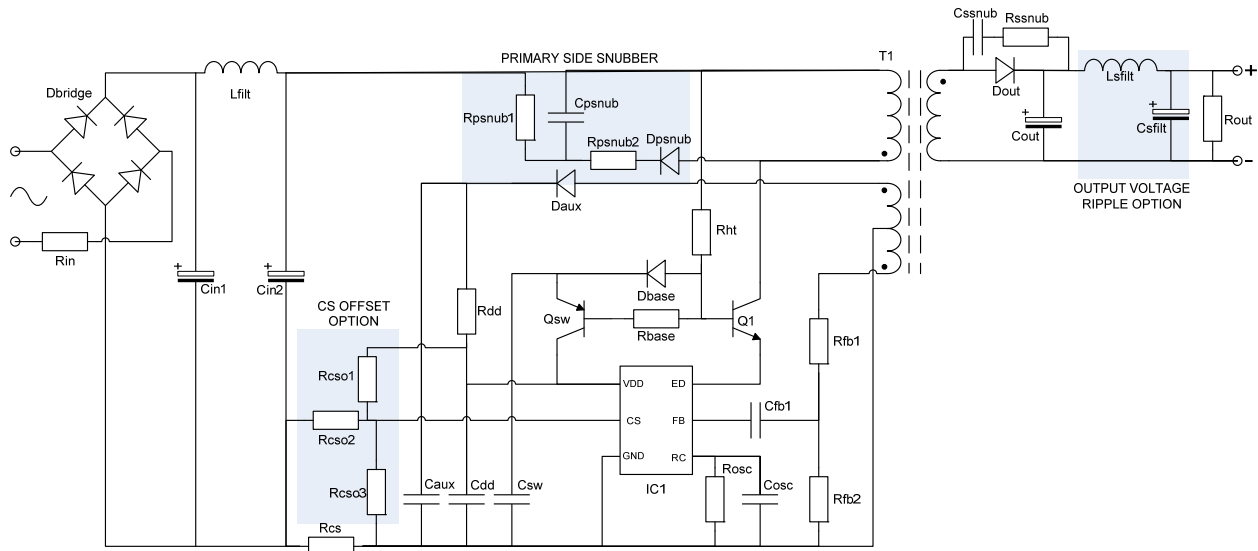


Figure 31: CS Offset Option Components

Choose $R_{cs} = 1 \Omega$ and R_{cso2} to be any value within the range 330 to $3.3 \text{ k}\Omega$, Calculate R_{cso3} according to the following formula:

$$R_{cso3} = R_{cso2} \cdot \left(\frac{R_{cs}}{1 - R_{cs}} \right)$$

Where R_{cs} is the value calculated in section 2.6.

It is also possible to slightly improve the accuracy of the constant current characteristic by adding resistor R_{cso1} to correct the small residual offset V_{CSOFF} . Calculate R_{cso1} according to the following formula:

$$R_{cso1} = \left(\frac{V_{DD}}{V_{CSOFF}} \right) \left(\frac{R_{cso2} \cdot R_{cso3}}{R_{cso2} + R_{cso3}} \right)$$

5.2 Reduced Output Voltage Ripple Option (Csfilt, Lsfilt)

To reduce output voltage ripple, two extra components can be added to form a π filter as shown in Figure 32.

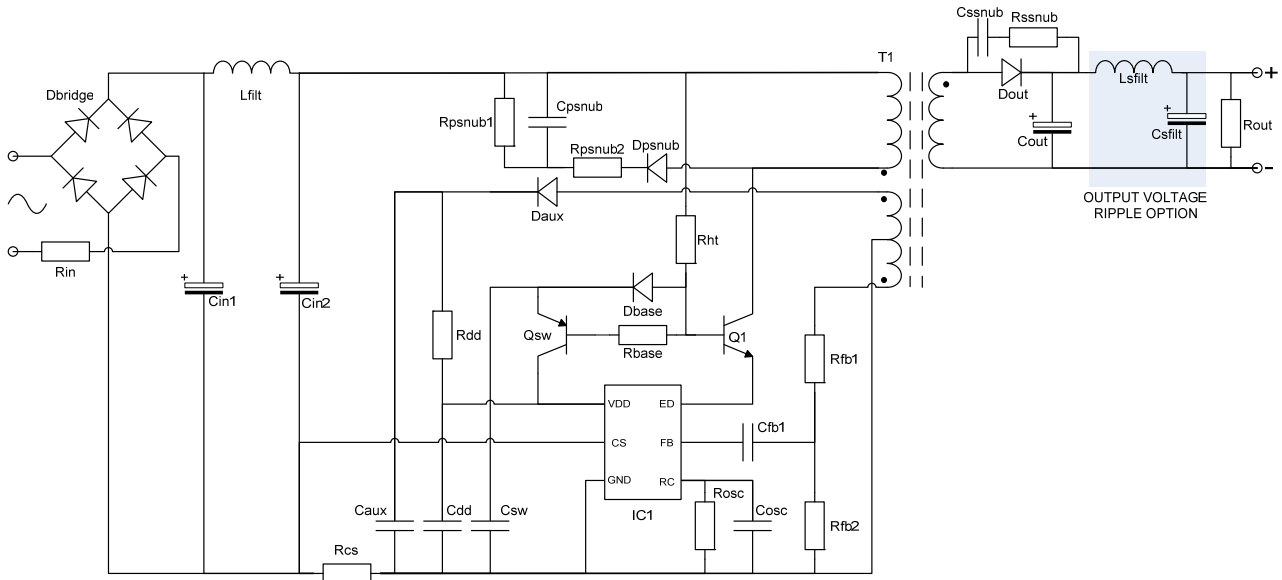


Figure 32: Output Voltage Ripple Option

Forming a π filter with Csfilt, Lsfilt and Cout reduces output switching ripple. The natural resonance of the π filter must be > 2 kHz to maintain the control loop phase margin. In applications with higher output currents, it is necessary to connect output capacitors in parallel to share the RMS ripple current, see section 2.8.2.

Csfilt can be 47 μ F but must have a working voltage greater than V_{NOM} . Lsfilt can be 10 μ H.

5.3 Reduced Collector Voltage Option (Rpsnub1, Rpsnub2, Cpsnub, Dpsnub)

If the peak collector voltage is an issue, a primary snubber can be added as shown in Figure 33. Cpsnub, Rpsnub1, Rpsnub2 and Dpsnub form a simple diode clamping snubber.

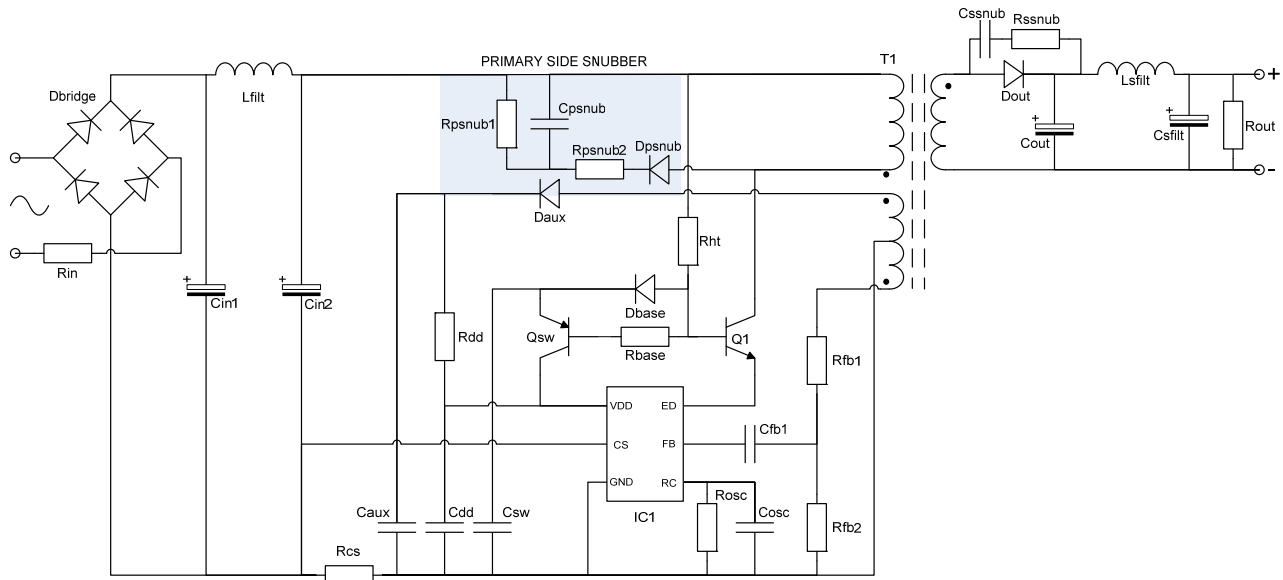


Figure 33: Primary Snubber Components

Cpsnub can be 470 pF with a 500 V rating.

A 1N4007GP diode is recommended for Dpsnub; alternatively, faster diodes such as HER107, FR107 may be used; slower types, such as the 1N4007 (without GP suffix) may be used provided that the value of Rpsnub2 is chosen to be > 200 Ohms, to ensure that the reverse recovery time is small enough.

Rpsnub1 can be chosen in the range of 150 kΩ to 1 MΩ; a trade-off between efficiency and peak collector voltage needs to be made.

Rpsnub2 can be chosen in the range of 22 Ω to 1 kΩ; a trade-off between peak collector voltage and RF emissions compliance needs to be made.

Note that adding the primary snubber will change the calculated value for Caux (in section 2.7.1).

5.4 Simplified Transformer Design for 1-3 W Applications

For 1-3 W applications, it is possible to have a simplified transformer option as shown by the WT1 winding configuration. This may suffer from less EMI margin and larger output voltage ripple.

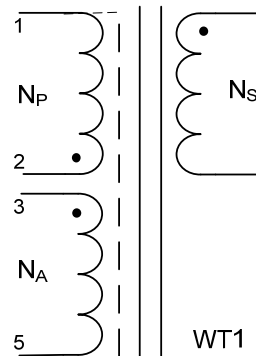


Figure 34: Transformer Schematics for Simplified WT1 Winding Topology

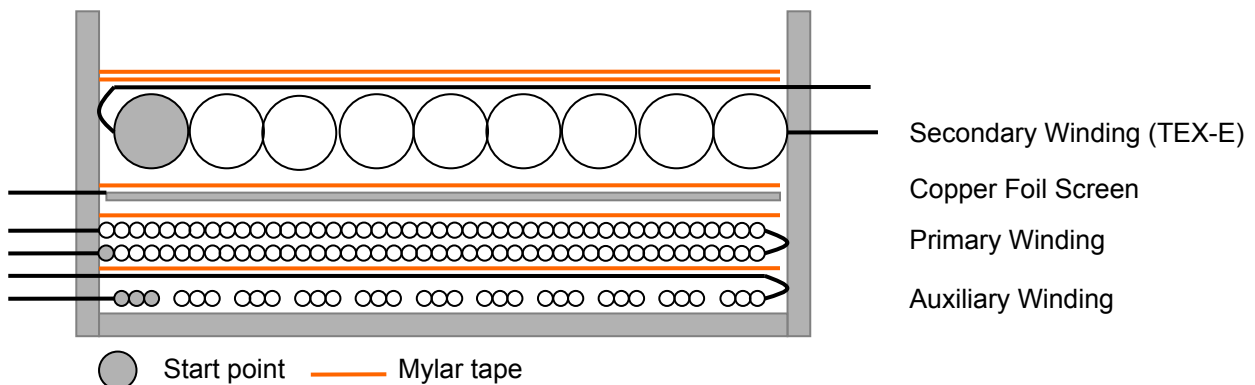


Figure 35: WT1 Transformer Winding Arrangement

WT1 Winding	Type	Wire	Wire Turns	Wire Layers	Tape Turns
W1	Auxiliary	3 x 0.23 mm ECW	7	1	1
W2	Primary	1 x 0.12 mm ECW	160	3	1
W3	Screen	7 x 28 mm Cu foil	1	1	1
W4	Secondary	See Table 7			2
W5	Flux-band	1 x 0.2 mm TCW	2	1	0

Table 20: WT1 Transformer Winding Configuration

6 TESTING AND TROUBLESHOOTING YOUR DESIGN

Once the components are selected and the transformer constructed a prototype of the design can be made. This section provides first steps in testing and observing behaviour of your application design. It also provides some trouble shooting advice. Refer to the controller datasheet (reference DS-2918) for further information about the ICs and their operating modes.

6.1 Safety

Offline power supply prototypes may exhibit safety hazards including, but not limited to, electric shock, high temperatures, fire and smoke. Indeed, some standard procedures deliberately take the unit under test to the point of destruction. Prototypes should be tested and worked on only by competent and suitably trained personnel. The following general advice is offered but cannot take account of risks associated with any particular prototype or test set up. If you are in any doubt as to the safety of any unit or test procedure, please consult a competent adviser before proceeding.

- Before operating the unit:
 - Ensure that the documentation matches the unit to be tested and familiarise yourself with both. If there is a discrepancy or any doubt do not proceed with testing but contact your CamSemi representative for assistance;
 - Prototypes are often modified in the course of development. Check the unit to be tested for design or build errors before connecting it to the supply. Only proceed if you are satisfied that the unit is as intended and in a suitable condition for the testing to be performed;
 - Ensure general safety of the test set-up. For example, minimise the risk of inadvertent contact with the unit under test and injury from material which may be ejected from it in the event of a "catastrophic" failure;
- While operating the unit:
 - Do not connect the unit direct to the mains utility. Use a suitable isolated supply for the type of unit and the tests to be performed;
 - Remember that insulation between high voltage and low voltage parts of a prototype may not provide full safety isolation;
 - Regard all parts of the unit as potentially LIVE and HAZARDOUS;
- After disconnecting the supply:
 - Hazardous voltages will persist for some time after the supply is disconnected due to charge stored in capacitors. If necessary, capacitors can be safely and quickly discharged using a suitable resistor.
- Allow the unit to cool before handling it.

6.2 First Power-up (100% Load)

Attach a high voltage oscilloscope probe to the collector of the primary switch (Q1). Apply universal mains input voltage with 100% load on the output. Observe the collector voltage waveform. It should be similar to the oscilloscope plot in Figure 36.



Figure 36: Q1 Collector Voltage Waveform with 100% Load

If no switching signal is observed, check the primary side components for connectivity and correct polarity.

6.3 Typical Controller Waveforms

Figure 37 shows some typical waveforms that can be observed on the pins of the CamSemi controller chip.

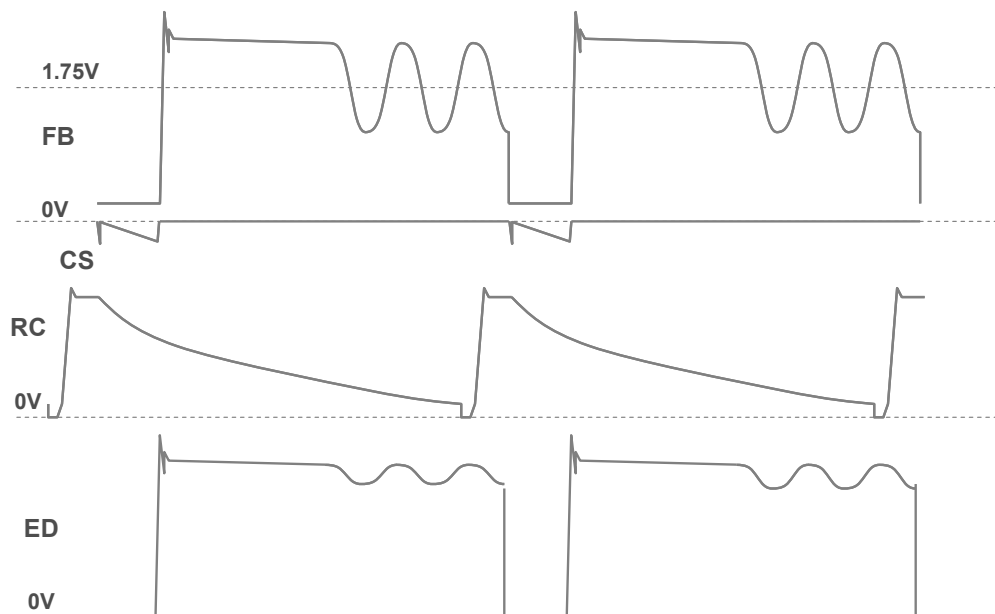


Figure 37: Typical Controller Waveforms

6.4 Troubleshooting

6.4.1 Unit hiccups but cannot start

- Ratio of Cout/Cdd too high
 - Increase Cdd (NB:Y5V capacitors need higher voltage rating to deliver capacitance)
 - Optimum ratio given by $Cdd > Cout * (V_{NOM}/I_{NOM})/1000$
- Auxiliary power winding not tightly coupled to primary winding
 - Decrease leakage to auxiliary winding
- Slow Daux rail diode
 - Use Daux diode with $TRR \leq 50ns$
- Not enough leakage inductance (between primary and secondary)
 - Increase separation between primary and secondary windings

6.4.2 Unstable output at low/no load

- Poor quality of FB waveform
 - Improve secondary/auxiliary coupling to reduce transformer ringing
 - Add feedback winding (enhancement to design in 5.4, see 2.3.5)
- Output (load) capacitance too large
 - Reduce output (load) capacitance

6.4.3 Voltage rises at no-load

- Caux value incorrect
 - Check for Double Punch (Reduce Caux)
 - Controller issues single pulses only (Increase Caux)
- No-load power too high (See section 6.4.4 below)
- Inadequate dummy load
 - Reduce value of Rout

6.4.4 No-load power too high

- Caux value incorrect
 - Check for Double Punch (Reduce Caux)
 - Controller issues single pulses only (Increase Caux)
- Increase value of Rbase
- Increase value of Rht (check that start-up time is OK)
- Increase Rout (check that output does not rise at no load, high line)

6.4.5 Primary switch gets too hot

- Adjust value of Rbase
- Use higher current BJT for Q1

6.4.6 Collector voltage peak is too high

- Improve primary/auxiliary coupling
- Reduce Bmax on transformer
- Use secondary snubber (described in 2.8.4)
- Add primary snubber (enhancement described in 5.3)
- User higher voltage transistor for Q1 (e.g. STX616, TS13003MV)

6.4.7 ED pin peak voltage too high

- Try a different type of transistor for Q1
- Try a different type of diode for Dbase

6.4.8 Poor efficiency at low line voltage

- Decrease value of Rbase
- Select higher current BJT for Q1

6.4.9 Poor efficiency at high line voltage

- Reduce primary/auxiliary coupling
- Improve primary/secondary coupling
- Decrease value of Rbase
- Use higher ripple current devices for output capacitors

6.4.10 High conducted emissions

- Adjust values of secondary snubber components
- Check transformer construction and / or use alternate type
- If using minimal configuration (section 2.9.1) use lower ESR type for Cin
- Increase current rating of Lfilt to check if the inductor is saturating
- Reduce track length attached to Q1 collector
- Try adding a fluxband (connected to a DC level) with an unvarnished core

6.4.11 High radiated emissions

- Add fluxband to transformer / check fluxband connection
- Try unvarnished transformer
- Add snubber to secondary diode
- Check the Daux – Caux – T1 loop is small
- Try different Daux
- Add small ferrite bead in series with Daux

6.4.12 Failing 2nd harmonic 900 MHz emissions test

- Add 33 pF capacitor across Daux

6.4.13 Current limit accuracy

- Set CC limit by adjusting Rcs
- Add CS offset correction (enhancement described in 5.1) to reduce line voltage variation
- Improve VDD decoupling by using ceramic type capacitor for Cdd and shorter PCB traces
- Check for excessive dissipation in the auxiliary circuit
- Check to see if R_{DD} can be increased
- Try reducing transformer capacitance by adding tape between primary layers.

6.4.14 Output ripple too high in CV mode

- Add π -filter (enhancement described in 5.2)
- And/or add second output capacitor (described in 2.8.2)

6.4.15 Input power too high in short-circuit

- Charger does not enter foldback in short-circuit condition
 - Reduce primary/auxiliary coupling
 - Or improve primary/secondary coupling
- Bootstrap supplying too much current (at high line voltage)
 - Increase value of Rht1, Rht2

6.4.16 Output voltage drops at high line voltage

- Input over voltage protection triggering too early
 - Adjust secondary snubber to reduce undershoot on controller FB pin
 - Slightly increase primary turns, N_P

7 EXAMPLE APPLICATION DESIGN

7.1 Application Design Parameters

Table 21 is the target specification for the application design example.

Design Parameter	Symbol	Typical Range Achievable	Typical Value Using this Design Guide	Comments
Nominal output power	P_{NOM}	1 to 8 W	4.8 W	Nameplate is 4 W
Nominal output voltage	V_{NOM}	3 to 24 V	6 V	Nameplate is 5 V
Nominal output current	I_{NOM}	0.1 to 2.5 A	800 mA	Same as I_{CCMIN}
Output voltage tolerance	K_{CVTOL}	< 10%	10%	
Output current tolerance	K_{CCTOL}	< 15%	10%	
Cable compensation	G_{CAB}	1 to 10%	2%	
Nominal switching frequency at full load	F_{NOM}	40 to 65 kHz	60 kHz	Operating frequency at maximum load
Input voltage	V_{AC}	85 to 265 Vac	90 to 265 Vac	Universal input
Input voltage frequency	F_{AC}	45 to 66 Hz	50 Hz	
Input voltage withstand		0 to 85 Vac and 265 to 300 Vac	0 to 90 Vac and 265 to 300 Vac	
Rectified input voltage	V_{DC}	80 V to 375 V	80 V to 375 V	
Average system efficiency	η_{NOM}	63% to 85%	$\geq 68.5\%$	EPS 2.0 plus 2% margin
No-load power consumption	P_{NL}	< 150 mW	< 30 mW	Five star charger
Transformer inductance tolerance	K_{LPTOL}	0 to $\pm 15\%$	$\pm 10\%$	
Conducted emissions EN55022 class B	-	Compliant with margin	Compliant with 6 dB margin	
Maximum duty cycle	D_{MAX}	50%-60%	50%	
Nominal duty cycle	D_{NOM}	Defined by D_{MAX}	45%	
DC brown-out voltage	V_{DCBRN}	65 V to 75 V	70 V	
Auxiliary voltage	V_{AUX}	4 V to 5 V	4 V	
Q1 turn-off time	t_{BJTOFF}	100 ns to 400 ns	200 ns	BJT storage time
Output diode forward voltage	V_{DF}	0.25 V (schottky) 0.65 V (epitaxial)	0.25 V	
Base-emitter forward voltage	V_{BE}	0.65 V	0.65 V	
Transformer resonance frequency (in-circuit)	F_{RES}	> 300 kHz	400 kHz	
Feedback adjustment factor	t_{FB}	70 ns	70 ns	
Short-circuit power consumption		< 1 W	< 1 W	
Turn-on delay		< 1 s	< 1 s	
Transient response output deviation		< 10%	< 10%	Output voltage for 0-100-0% load change

Table 21: Design Example Specification

7.2 Components Selected Using Design Guide

Table 22 summarises the components in the example determined using the design guide.

Block	Components	Design Guide	Selected Type / Value	Comments
Input Rectifier and Filter	Dbridge	See section 2.1.1	MBS6	Diode bridge with small footprint
	Rin	See section 2.1.2	10 Ω	
	Lfilt	See section 2.1.3	330 μ H	
	Cin1	See section 2.1.4	4.7 μ F 400 V	
	Cin2	See section 2.1.4	4.7 μ F 400 V	
Switch	Q1	See section 2.2.1	STX616	
	Rbase	Section 3.3 / 4.1.5	150 Ω	
	Dbase	Section 3.1 / 4.1.3	TS4148	ED pin voltage checked and ok
	Qsw	See section 4.1.1	BCX17	
	Csw	See section 4.1.2	220 nF X7R 16V	Cheaper than 470 nF
Transformer	T1 Winding Topology	See section 2.3	WT3	
	Core/Bobbin		EFD15	Headroom limited
	Primary Inductance		2.15 mH	
	Primary Winding		104 + 56	Easier split to wind
	Secondary Winding		10	Regulates at 6 V
	Auxiliary Winding		7	
	Feedback Winding		5	Regulates at 6 V
	Other (fluxband, screen)		Fluxband	
Controller	IC1	See section 2.4.1	C2162PX2	
	Cosc	See section 2.4.2	1 nF	minimum cable compensation due to wide voltage region
	Rosc	See section 2.4.2	47 k Ω	
Feedback	Rfb1	See section 2.5.1	910 Ω 20 k Ω	Adjusted to improve voltage regulation point
	Rfb2	See section 2.5.1	130 Ω	
	Cfb	See section 2.5.2	47 nF	
Current Sense	Rcs	See section 2.6.1	1 Ω	Easier to source
	Rcso1	See section 5.1	NF	
	Rcso2		1 k Ω	To allow a 1 Ω resistor to be used for Rcs
	Rcso3		1.2 k Ω	
VDD and Auxiliary	Rht	Section 3.2 / 4.1.4	27 M Ω	Easy to source
	Caux	See section 2.7.1	3.3 μ F 10% X5R 16V	
	Daux	See section 2.7.2	STTH1R02	
	Cdd	See section 2.7.3	2.2 μ F X7R 10% 10V	
	Rdd	See section 2.7.4	220 Ω	Lowest value with ok ripple
Output	Dout	See section 2.8.1	MBRS2040	20% derating V_{RRM}
	Cout	See section 2.8.2	2 x 470 μ F	To reduce voltage ripple
	Rout	See section 2.8.3	10 k Ω	Improved no-load power, V mask allows for voltage lift
	Cssnub	See section 2.8.4	4.7 nF	
	Rssnub	See section 2.8.4	4.7 Ω	

	Csflt	See section 5.2	NF	
	Lsflt		NF	
Primary snubber option	Rpsnub1	See section 5.3	NF	
	Rpsnub2		NF	
	Cpsnub		NF	
	Dpsnub		NF	

Table 22: Design Example Components

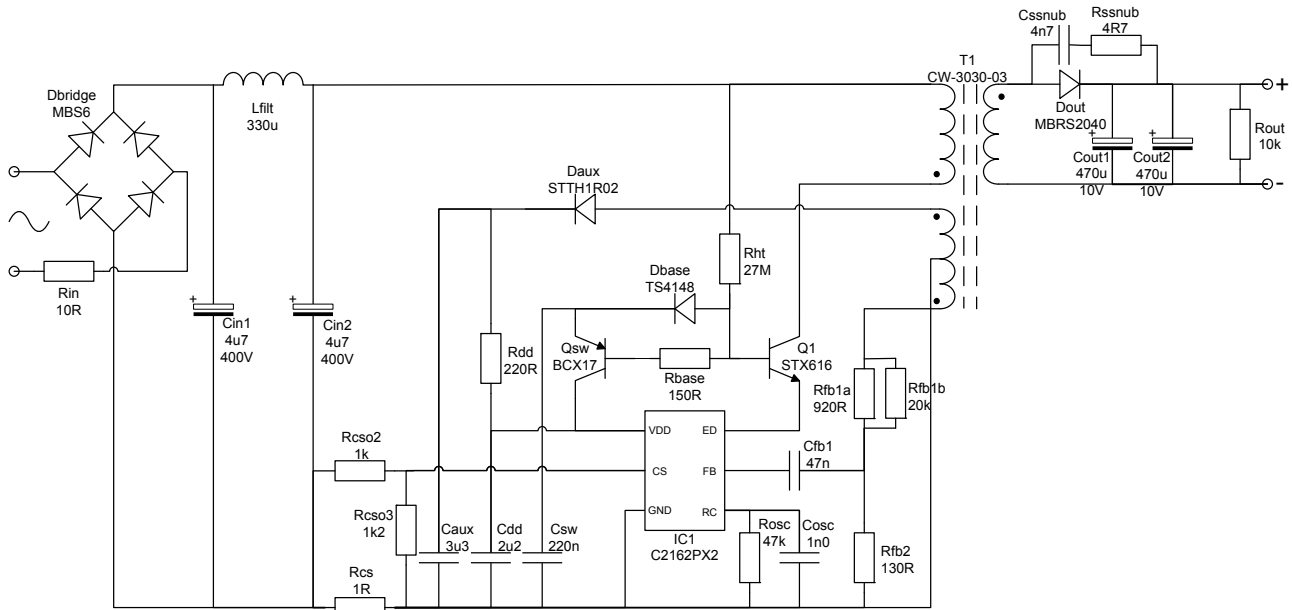


Figure 38: Design Example Schematic

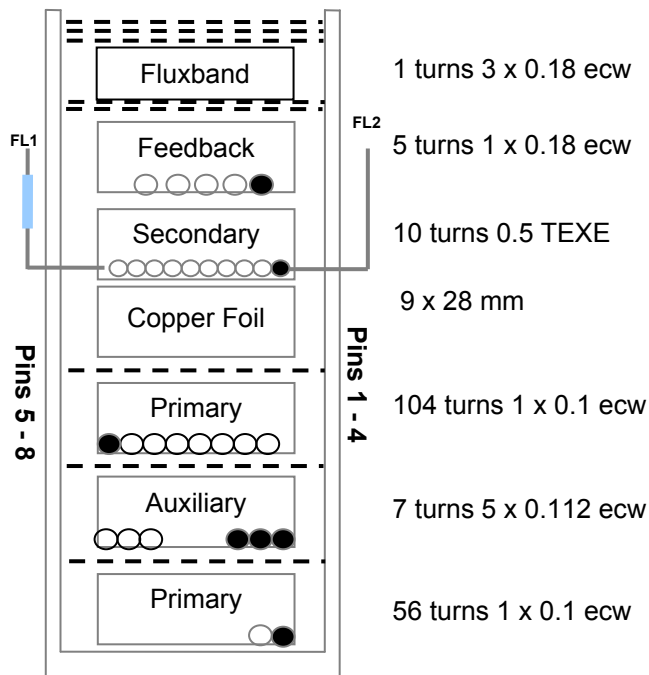


Figure 39: Design Example Transformer (CW-3030-03)

7.3 Measured Performance

7.3.1 Output CV/CC Characteristic

The following VI characteristic was measured at the end of the cable. The minimum of 2% cable compensation has been applied because the voltage regulation region is wide.

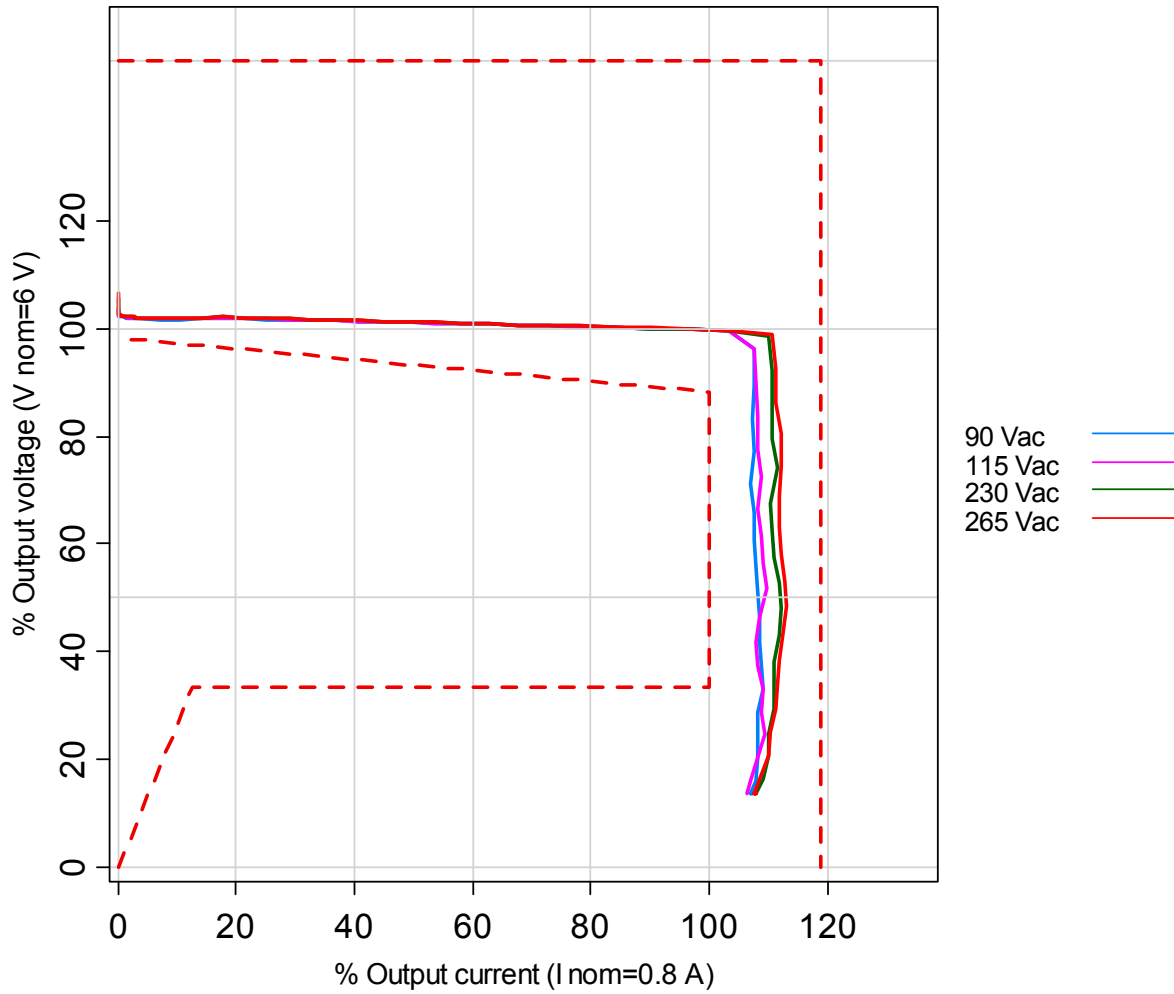


Figure 40: V-I Characteristics

7.3.2 Conversion Efficiency

Average efficiency was 75% at room temperature as shown below. Limits assume a nameplate power of 4 W (5 V / 0.8 A).

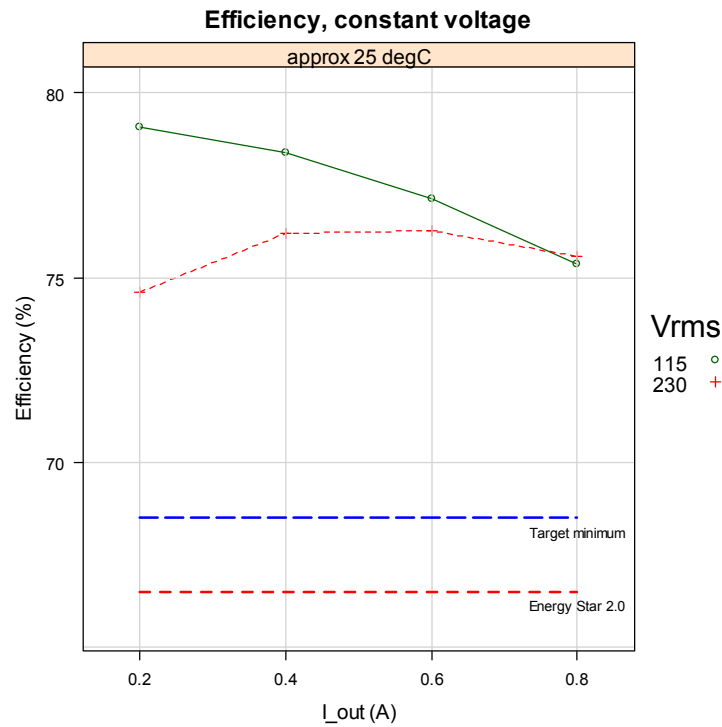


Figure 41: Efficiency Measurements

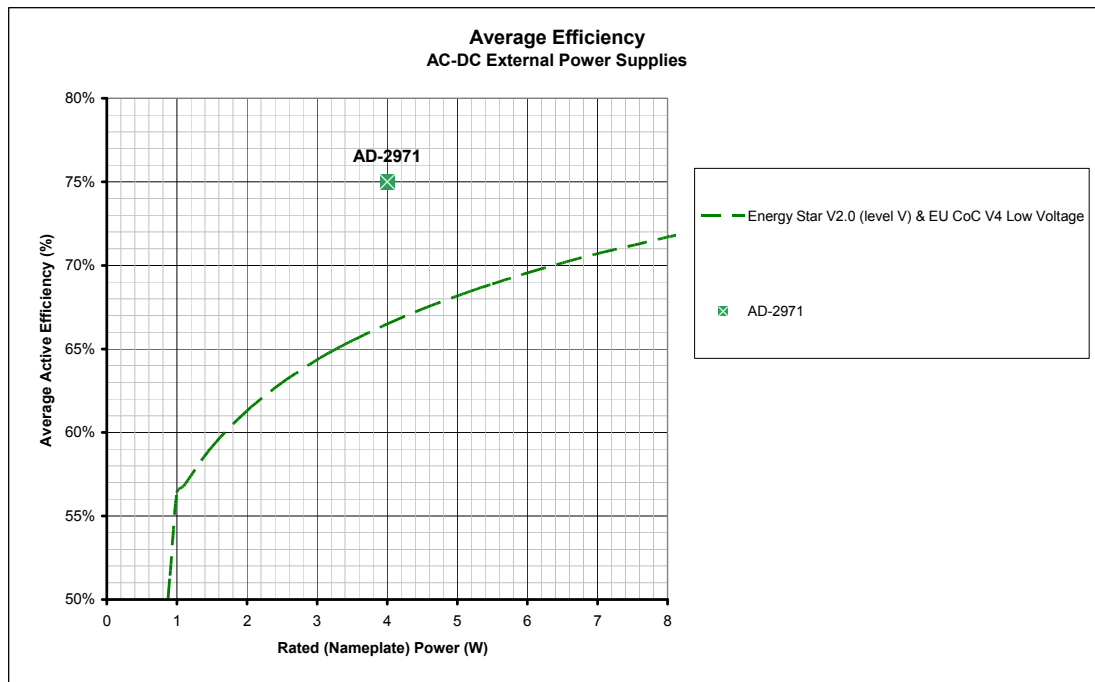


Figure 42: Comparison Average Efficiency with Standards

7.3.3 No-Load Power Consumption

No-load power consumption was 23 mW. A nameplate power of 4 W (5 V / 0.8 A) is assumed.

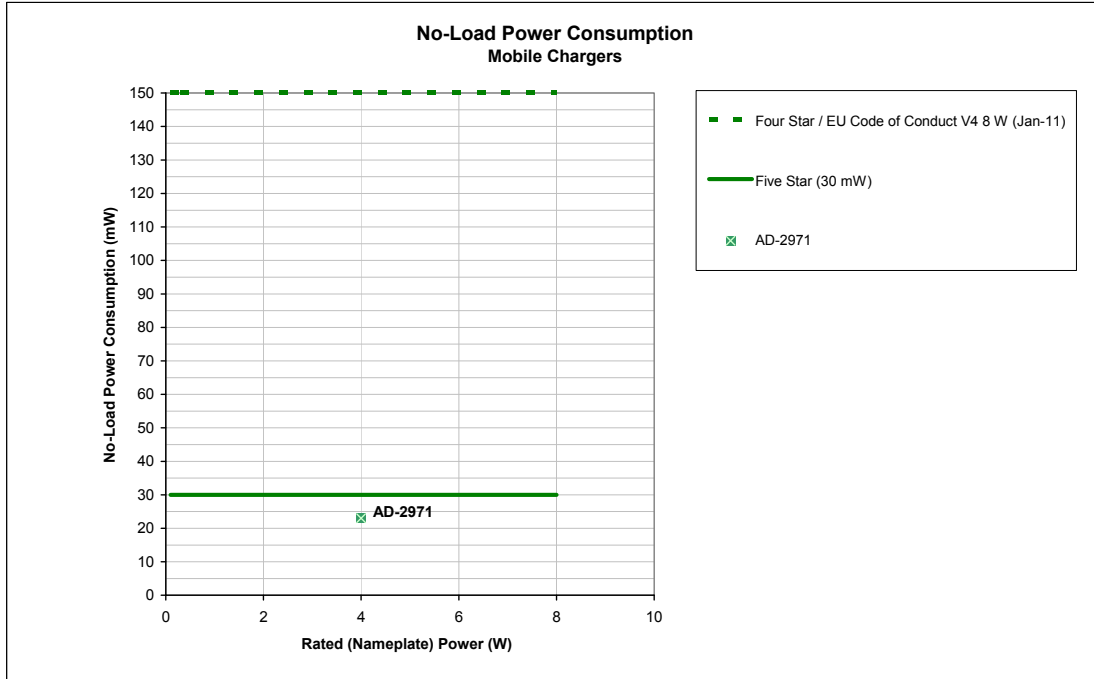


Figure 43: No-load Power Consumption

Temperature (°C)	Vin	No load power (mW)
approx 25	230	23
approx 25	115	16

Table 23: No-load Power Results

7.3.4 Short-Circuit Power Consumption

Table 24 shows short circuit power consumption measurements at room temperature.

Temperature (°C)	Vin	Short circuit power (W)
25	115	0.244
25	230	1

Table 24: Short Circuit Power Results

7.3.5 Start-Up

The output voltage rise was measured driving into a resistive load representative of full power after the application of mains input voltage. With 115 Vac input, the output voltage is established and regulated within 250 ms of mains being applied. With minimum input voltage supplied, the unit starts up in less than 1 s.

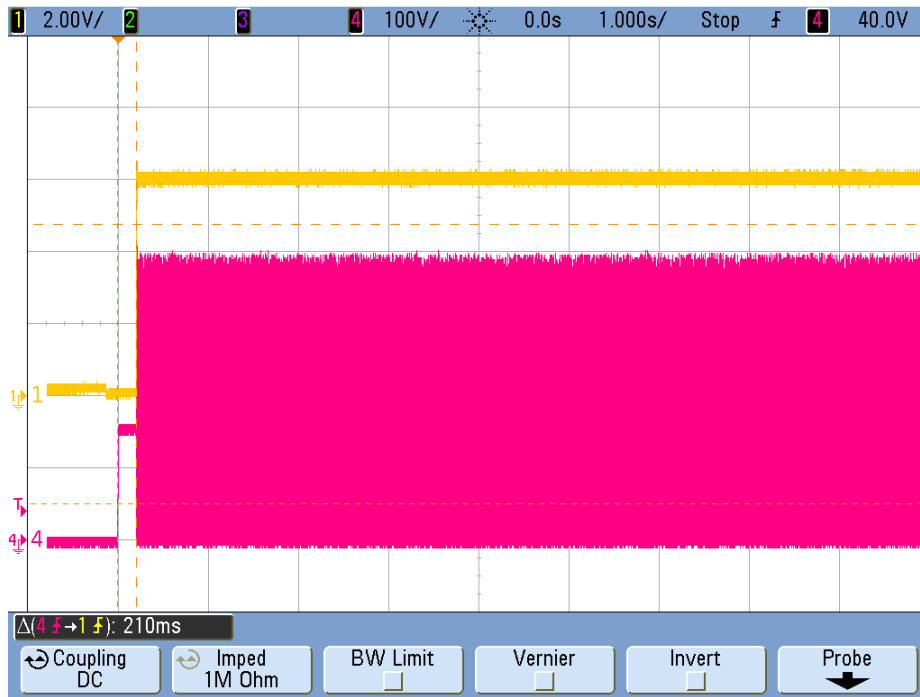


Figure 44: Start-up Scope Plot (115 Vac)

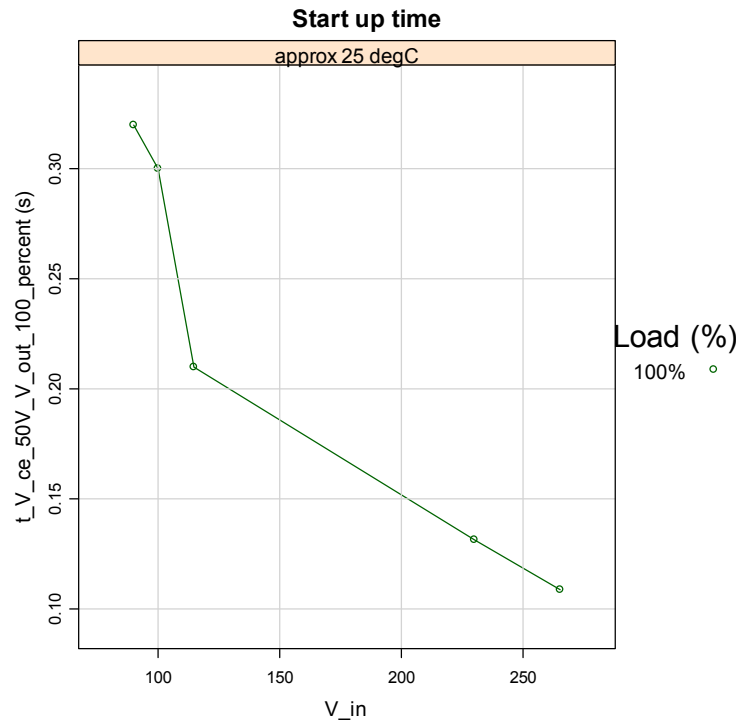


Figure 45: Start Up Time Variation with Mains Voltage

7.3.6 Transient Response: 0% to 100% Load Step

In Figure 46 Channel 1 is Vout, Channel 3 is Iout. Input voltage is 230 Vrms. Load step is constant voltage load, no load to 4 V. The recovery time is less than 10 ms.

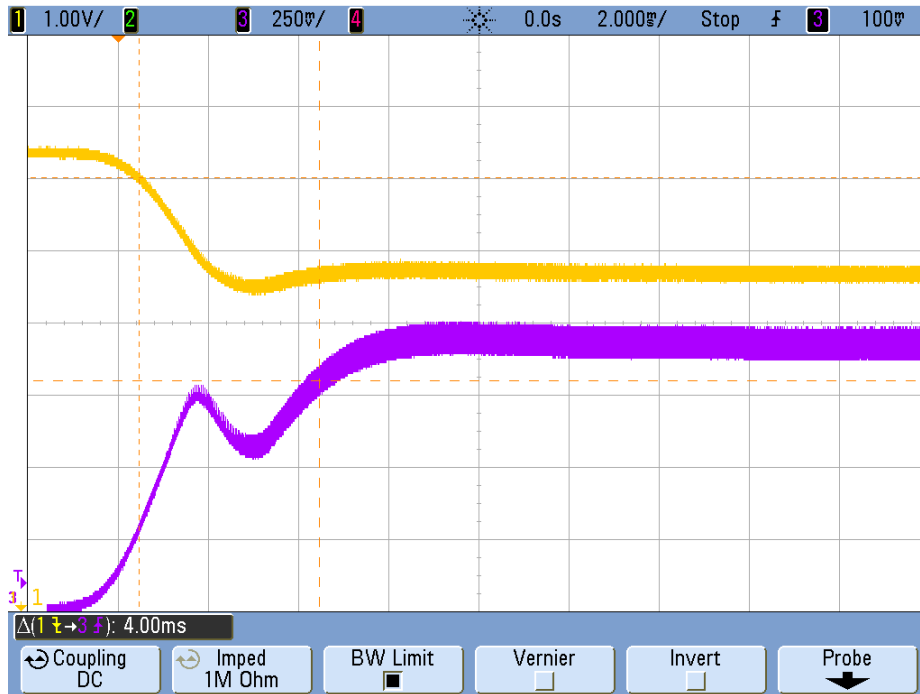


Figure 46: 0% to 100% Load Step Transient

Vin (rms)	T (°C)	Maximum recovery time (ms)
115	25	4.06
230	25	3.99

Table 25: 0% to 100% Load Step Recovery Time

7.3.7 Collector Voltage

Figure 47 shows the maximum collector voltage seen is approximately 600 V.

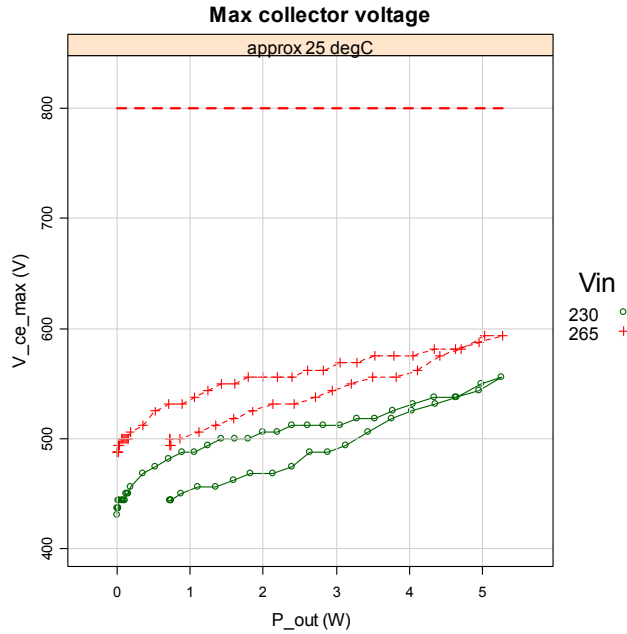


Figure 47: Maximum Collector Voltage

7.3.8 Operating Frequency

Figure 48 shows the variation of switching frequency with load and mains input voltage around the VI mask. The maximum is frequency seen is approx 60 kHz.

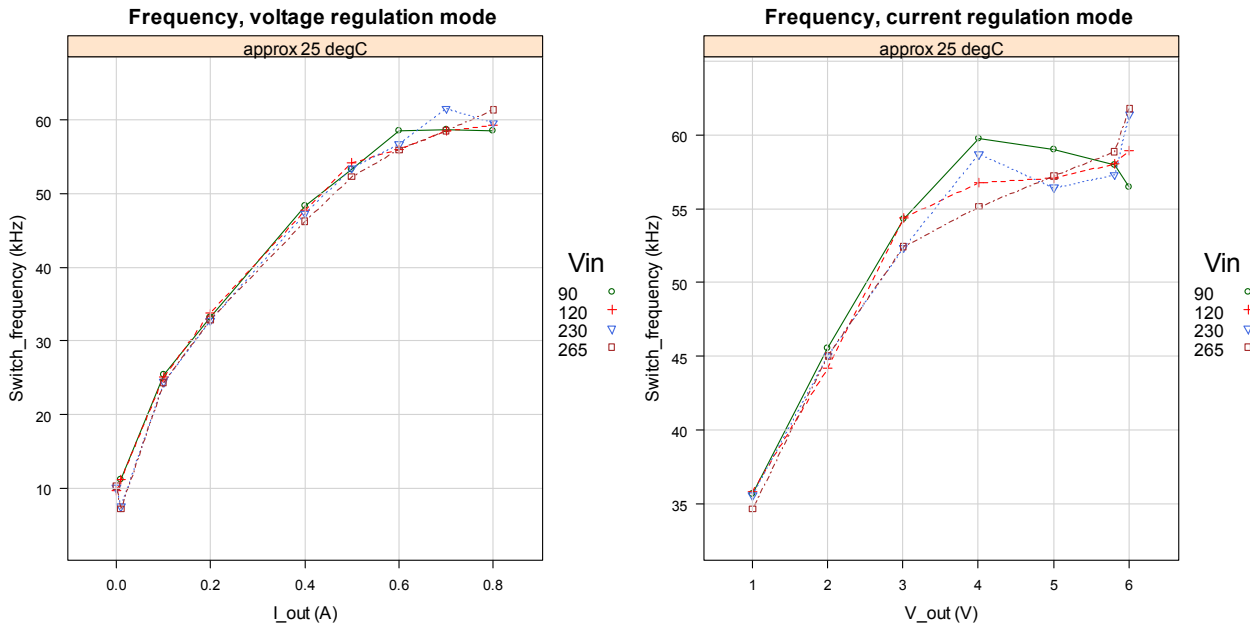


Figure 48: Switching Frequency Variation

7.4 Voltage Ripple

The red lines in the following graphs indicate the upper limits of the target specification requirements.

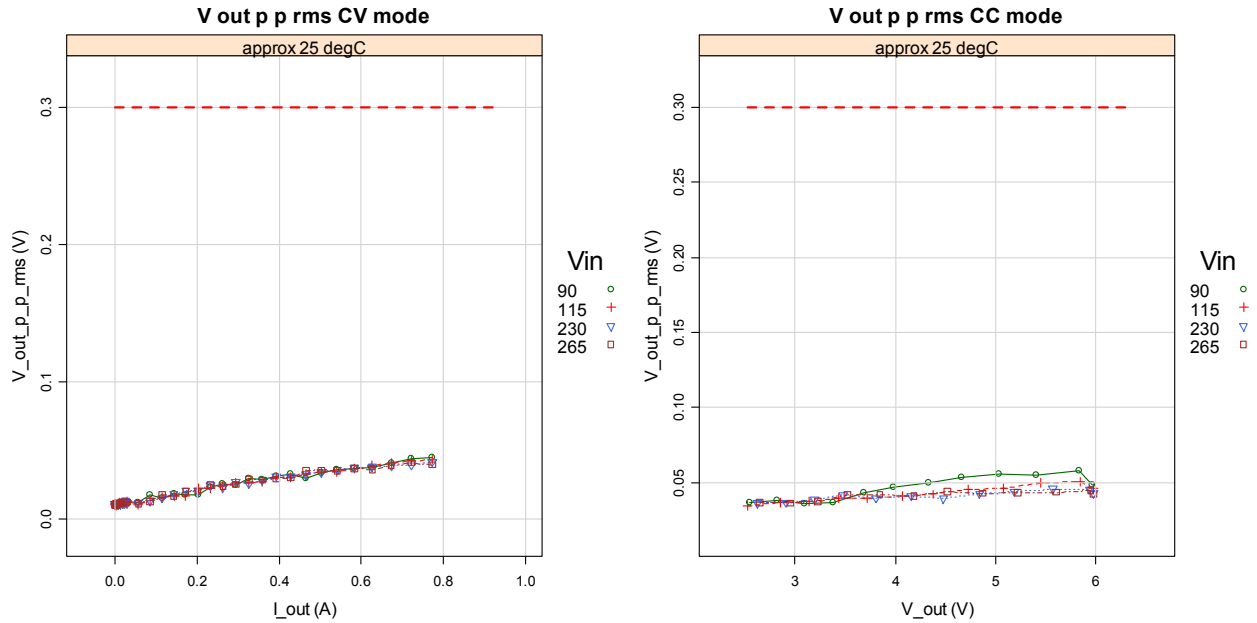


Figure 49: Peak to Peak RMS Output Voltage Ripple in CV and CC Mode

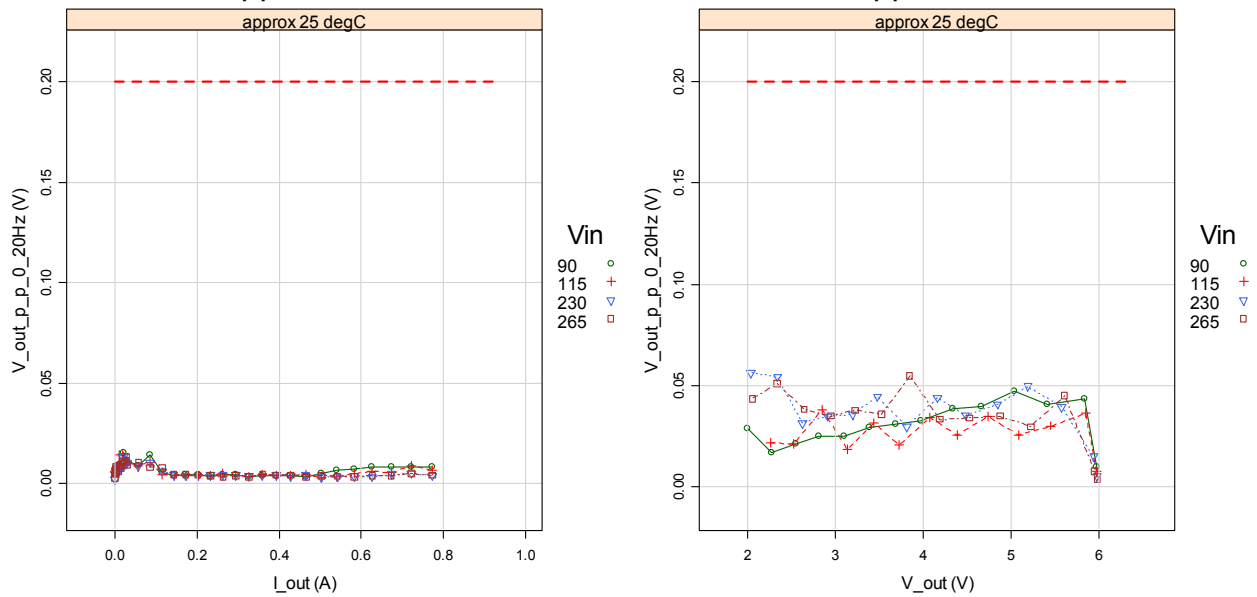


Figure 50: Output Voltage Ripple in CV and CC Mode Between 0 Hz and 20 Hz

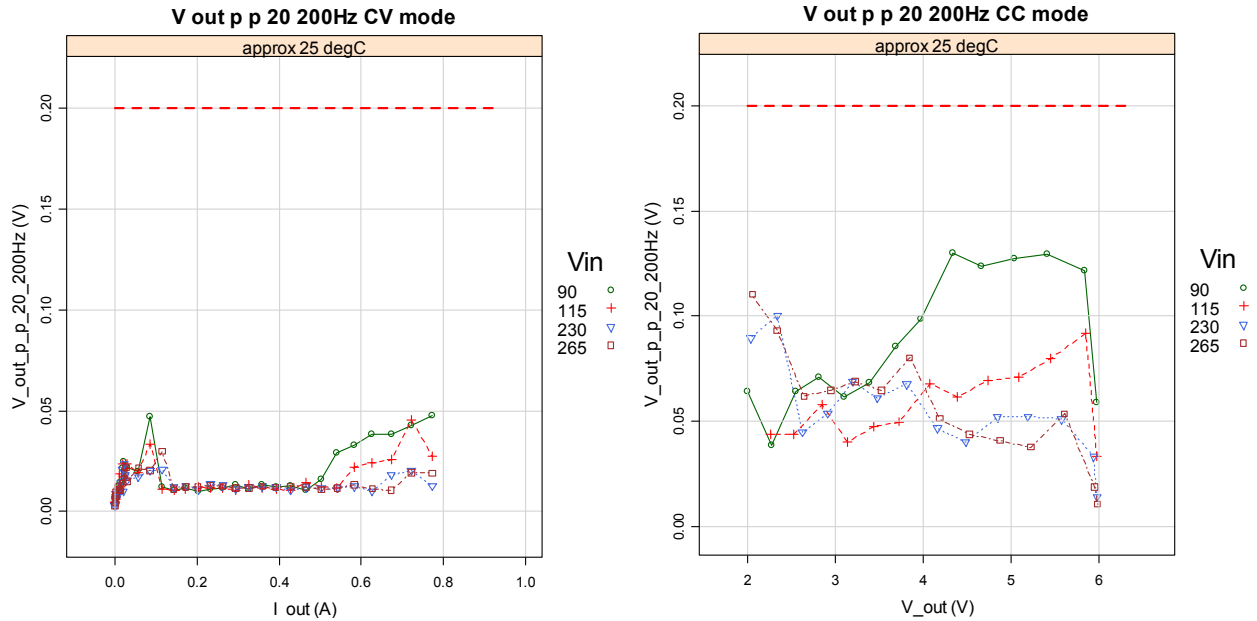


Figure 51: Output Voltage Ripple in CV and CC Mode Between 20 Hz and 200 Hz

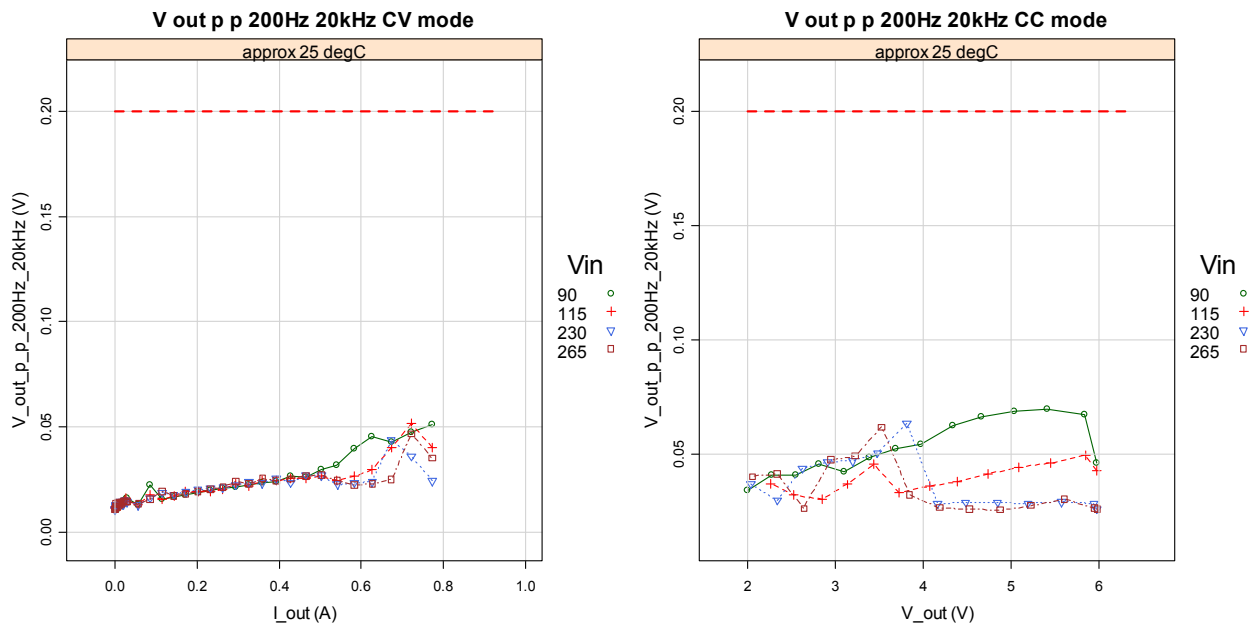


Figure 52: Output Voltage Ripple in CV and CC Mode Between 200 Hz and 20 kHz

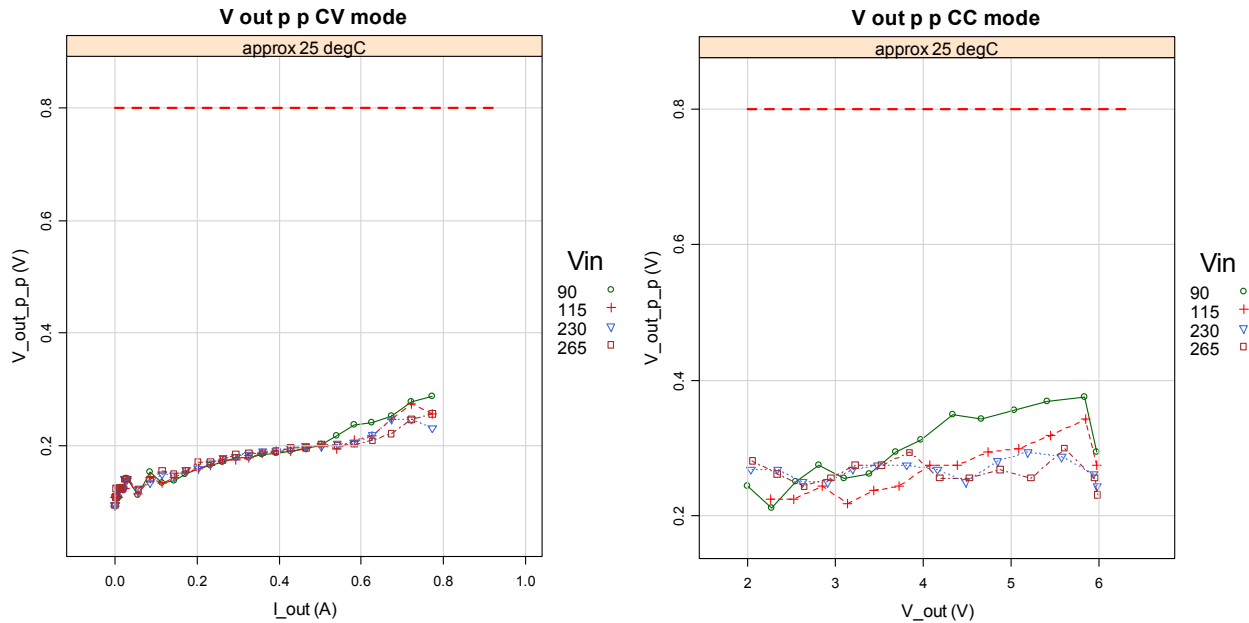


Figure 53: Peak to Peak Output Voltage Ripple in CV and CC Mode

7.4.1 Conducted EMI Measurements

Conducted EMI was measured at 230 Vac in live and neutral phases with the output ground connected to earth to represent worst-case common-mode noise. The output load was a resistor representative of maximum output power. Worst case EMI was measured in the neutral line and showed a 6 dB margin

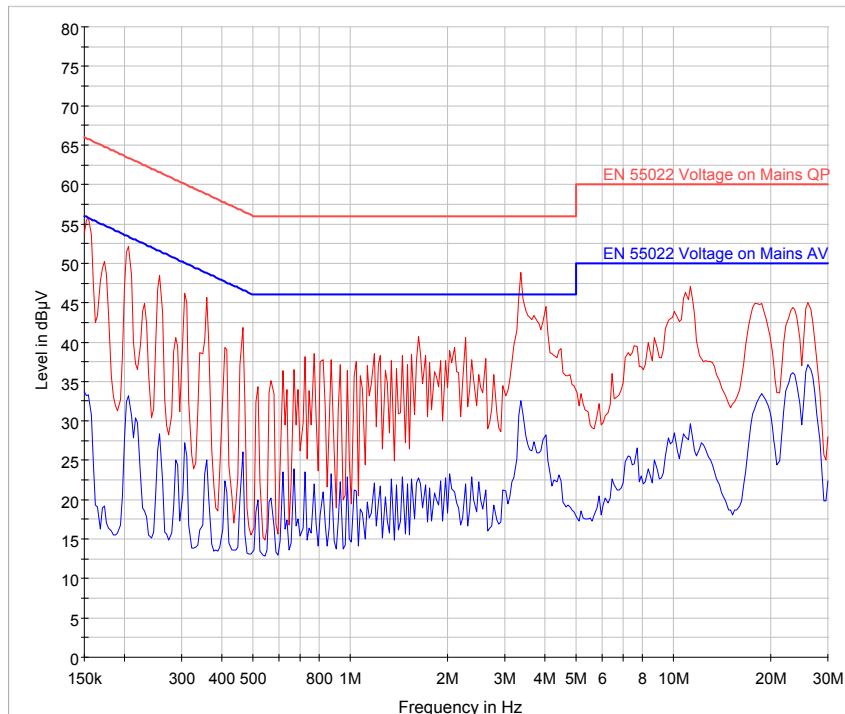


Figure 54: Application Conducted EMI (Line 1)

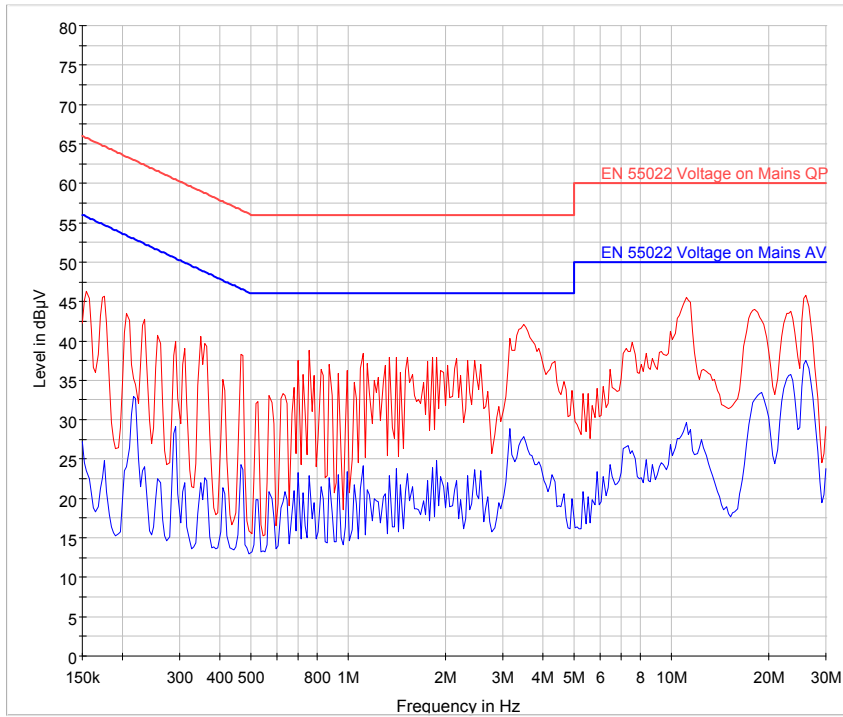


Figure 55: Application Conducted EMI (Line 2)

APPENDIX A DESIGN WORKSHEET

The following worksheets can be used when designing a PSS design with this design guide.

A.1 Specify Your Design Parameters

Use Table 26 to record your basic design parameters.

Design Parameter	Symbol	Typical Range Achievable	Target Value	Comments
Nominal output power	P_{NOM}	1 to 8 W		
Nominal output voltage	V_{NOM}	3 to 24 V		
Nominal output current	I_{NOM}	0.1 to 2.5 A		
Output voltage tolerance	K_{CVTOL}	< 10%		
Output current tolerance	K_{CCTOL}	< 15%		
Cable compensation	G_{CAB}	2 to 10%		
Nominal switching frequency at full load	F_{NOM}	40 to 65 kHz		
Input voltage	V_{AC}	85 to 265 Vac		
Input voltage frequency	F_{AC}	45 to 66 Hz		
Input voltage withstand		0 to 85 Vac and 265 to 300 Vac		
Rectified input voltage	V_{DC}	80 V to 375 V		
Average system efficiency	η_{NOM}	63% to 85%		
No-load power consumption	P_{NL}	< 150 mW		
Transformer inductance tolerance	K_{LPTOL}	15%		
Conducted emissions EN55022 class B	-	Compliant with margin		
Maximum duty cycle	D_{MAX}	50%-60%		
Nominal duty cycle	D_{NOM}	Defined by D_{MAX}		
DC brown-out voltage	V_{DCBRN}	65 V to 75 V		
Auxiliary voltage	V_{AUX}	4 V to 5 V		
Q1 turn-off time	t_{BJTOFF}	100 ns to 400 ns		
Output diode forward voltage	V_{DF}	0.25 V (schottky) 0.65 V (epitaxial)		
Base-emitter forward voltage	V_{BE}	0.65 V		
Transformer resonance frequency (in-circuit)	F_{RES}	> 300 kHz		
Feedback adjustment factor	t_{FB}	70 ns		

Table 26: Design Parameters

A.2 Select Components Using Design Guide

Use Table 27 to record the components recommended by the guide for your target design parameters.

Block	Components	Design Guide	Selected Type / Value
Input Rectifier and Filter	Dbridge	See section 2.1.1	
	Rin	See section 2.1.2	
	Lfilt	See section 2.1.3	
	Cin1	See section 2.1.4	
	Cin2	See section 2.1.4	
Switch	Q1	See section 2.2.1	
	Rbase	Section 3.3 / 4.1.5	
	Dbase	Section 3.1 / 4.1.3	
	Qsw	See section 4.1.1	
	Csw	See section 4.1.2	
Transformer	T1 Winding Topology	See section 2.3	
	Core/Bobbin		
	Primary Inductance		
	Primary Winding		
	Secondary Winding		
	Auxiliary Winding		
	Feedback Winding		
	Other (fluxband, screen)		
Controller	IC1	See section 2.4.1	
	Cosc	See section 2.4.2	
	Rosc	See section 2.4.2	
Feedback	Rfb1	See section 2.5.1	
	Rfb2	See section 2.5.1	
	Cfb	See section 2.5.2	
Current Sense	Rcs	See section 2.6.1	
	Rcso1	See section 5.1	
	Rcso2		
	Rcso3		
VDD and Auxiliary	Rht	Section 3.2 / 4.1.4	
	Caux	See section 2.7.1	
	Daux	See section 2.7.2	
	Cdd	See section 2.7.3	
	Rdd	See section 2.7.4	
Output	Dout	See section 2.8.1	
	Cout	See section 2.8.2	
	Rout	See section 2.8.3	
	Cssnub	See section 2.8.4	
	Rssnub	See section 2.8.4	
	Csfil	See section 5.2	

	Lsflt		
Primary snubber option	Rpsnub1	See section 5.3	
	Rpsnub2		
	Cpsnub		
	Dpsnub		

Table 27: Selected Components

A.3 Measure Performance of Your Design

Use Table 28 to record the measured performance of your design.

Parameter	Achieved Performance	Conditions
Voltage regulation		
Current regulation		
Average efficiency		Average of 25%, 50%, 75%, 100% load points
No-load power		
Short-circuit power		
Switching frequency		Over range of loads
Voltage ripple		
Current ripple		
Load transient overshoot		0 – 100 – 0%
Load transient undershoot		
Load transient recovery time		
Start-up time		
Start-up overshoot		
Maximum collector voltage		Measured around VI mask
Conducted emissions		

Table 28: Record Measured Performance Design

DESIGN GUIDE STATUS

Application design information and specifications provided in this Design Guide (e.g., circuit schematics, board layouts and custom wound component drawings) have not been fully developed for production and have not been subjected to safety or EMC approvals testing. Hence, design information contained herein should not be used for production without further development, verification, validation, approvals and certification appropriate for the intended application.

This Design Guide contains information relating to use of an IC product whose specification is subject to change without notice. Therefore, please always refer to the most current version of this document and the relevant IC product datasheet, available from your CamSemi representative or at www.camsemi.com.

CONTACT DETAILS

Cambridge Semiconductor Ltd
St Andrew's House
St Andrew's Road
Cambridge CB4 1DL
United Kingdom

Phone: +44 (0)1223 446450
Fax: +44 (0)1223 446451
Email: sales.enquiries@camsemi.com
Web: www.camsemi.com

DISCLAIMER

The product information provided herein is believed to be accurate and is provided on an "as is" basis. Cambridge Semiconductor Ltd (CamSemi) assumes no responsibility or liability for the direct or indirect consequences of use of the information in respect of any infringement of patents or other rights of third parties. Cambridge Semiconductor Ltd does not grant any licence under its patent or intellectual property rights or the rights of other parties.

Any application circuits described herein are for illustrative purposes only. In respect of any application of the product described herein Cambridge Semiconductor Ltd expressly disclaims all warranties of any kind, whether express or implied, including, but not limited to, the implied warranties of merchantability, fitness for a particular purpose and non-infringement of third party rights. No advice or information, whether oral or written, obtained from Cambridge Semiconductor Ltd shall create any warranty of any kind. Cambridge Semiconductor Ltd shall not be liable for any direct, indirect, incidental, special, consequential or exemplary damages, howsoever caused including but not limited to, damages for loss of profits, goodwill, use, data or other intangible losses.

The products and circuits described herein are subject to the usage conditions and end application exclusions as outlined in Cambridge Semiconductor Ltd Terms and Conditions of Sale which can be found at www.camsemi.com/legal.

Cambridge Semiconductor Ltd reserves the right to change specifications without notice. To obtain the most current product information available visit www.camsemi.com or contact us at the address shown above.