

Contents

1	COMPONENTS IN A TYPICAL LOW POWER RDFC APPLICATION DESIGN	3
2	APPLICATION DESIGN PARAMETERS.....	4
3	COMPONENT SELECTION	5
3.1	Line Rectifier (Dbridge) Selection	5
3.2	Input Capacitance ($C_{IN} = C_{in1} + C_{in2}$) Selection	5
3.3	Transformer Design.....	6
3.4	Output Capacitor (C_{out}).....	10
3.5	Primary Switch Transistor (Q1).....	10
3.6	Resonant Capacitor (C_{col}) and C_p Capacitor Selection.....	11
3.7	Output Diode (D_{out}) Selection	12
3.8	COL Pin Protection (R_{col}).....	12
3.9	Current Sense Resistors (R_2 and R_{cs}).....	13
3.10	AUX Pin Supply Resistor (R_{aux}).....	13
3.11	V_{DD} Feed Resistor (R_{dd}).....	14
3.12	Other Components.....	14
4	TESTING AND TROUBLESHOOTING YOUR DESIGN	15
4.1	Safety	15
4.2	Typical Low Power RDFC IV Characteristic	15
4.3	First Power-up (No Load) – Standby Mode	16
4.4	Running with P_{OUT} at About 25% of Rated Power	17
4.5	P_{OUT} Up to Rated Power – Continuous Normal Mode	18
4.6	P_{OUT} Above Rated Power - Overload Mode.....	19
4.7	Short Circuit Load - Foldback Mode.....	20
5	EXAMPLE APPLICATION DESIGN	21
5.1	Application Design Parameters.....	21
5.2	Components Selected Using The Design Guide	22
5.3	Measured Performance.....	23
5.4	Example Design - Circuit Schematic.....	24
5.5	Example Design – PCB Layout.....	25
5.6	Line-Frequency Ripple	26
5.7	Switching-Frequency Ripple	26
5.8	Efficiency	27
5.9	Load Pull-Up.....	27
5.10	Recovery from Short Circuit.....	28
5.11	Load Transient (I_{OUT} Step From 10 mA to I_{NOM}) With Max Load Capacitance.....	28
5.12	Load Transient (I_{OUT} Step From I_{NOM} to 10 mA) With Max Load Capacitance.....	29
5.13	Turn-on Delay With Max Load Capacitance	29
5.14	Operating Frequency (Plot of Q1 Collector Voltage) Measured in Normal Mode.....	30
5.15	Conducted Emissions (EN55022 Class B Limits) Pre-Compliance Test.....	30
APPENDIX A	DESIGN WORKSHEET	31
A.1	Safety	31
A.2	Specify Your Design Parameters.....	31
A.3	Select Components Using the Design Guide.....	32
A.4	Measure the Performance of Your Design.....	33

1 COMPONENTS IN A TYPICAL LOW POWER RDFC APPLICATION DESIGN

Table 1 lists the components in a typical low power RDFC application circuit. Some values and types are fixed for designs that can be created with this guide. Others will be determined by working through the guide (in the sections referenced in the “Type / Value” column).

Component	Description	Function	Type / Value
Low power RDFC IC	Low power RDFC controller IC	Resonant forward mode converter controller	C2471LX2 SOT23-6
Dbridge	Bridge rectifier	Rectification of the ac input voltage	See section 3.1
Cin1, Cin2	Input bulk capacitors	Reduction of line frequency ripple and differential mode EMI (by virtue of the pi filter behaviour)	See section 3.2
Lfilt	Inductor	Input filter – reduces differential mode EMI	See section 3.12
Transformer core		Isolation and forward mode voltage conversion	Section 3.3.1
Secondary turns & wire size			Sections 3.3.2 & 3.3.5
Primary turns & wire size			Sections 3.3.3 & 3.3.6
Auxiliary turns & wire size			Sec. 3.3.4 & 3.3.8
Leakage inductance			See section 3.3.7
Construction			See section 3.3.8
Cout	Output capacitor	Output voltage smoothing	See section 3.4
Q1	Primary Switch transistor	Primary power switch controlled by low power RDFC IC	See section 3.5
Ccol	Q1 collector coupling capacitor	Sets resonant frequency and senses Q1 collector voltage (used by low power RDFC control algorithm)	See section 3.6
Cp	Programming capacitor	Sets the Q1 collector saturation voltage threshold.	
Dout	Output rectifier	Secondary voltage rectification	See section 3.7
Dcol1, Dcol2	COL protection diodes	Protects COL pin from over-voltage transients	See section 3.8
Rcol	COL protection resistor	Protects COL pin from over-current transients	See section 3.8
Rcs	Current sense resistor	Sets overload protection threshold	See section 3.9
R2	OCPL programming resistor	Controls low power RDFC converter efficiency at low loads	See section 3.9
Raux	Base drive control resistor	Controls peak Q1 base drive current	See section 3.10
Rdd	VDD supply resistor	Limits the VDD current through auxiliary winding	See section 3.10
Fuse	Antisurge fuse	Provides protection against circuit failure	See section 3.12
Rfuse	Flameproof fusible Resistor	Limits inrush current and aids with surge immunity	See section 3.12
Rht	VDD supply resistor	Supplies VDD during Start-up mode	See section 3.12
Csnub	Snubber capacitor	To reduce EMI during output diode turn-off	See section 3.12
Rsnub	Snubber resistor	To reduce EMI during output diode turn-off	See section 3.12
Cdd	Ceramic VDD capacitor	Decouples the chip VDD supply	See section 3.12
Daux	Auxiliary rectifier	Rectifies auxiliary voltage	See section 3.12
Caux	Auxiliary capacitor	Decouples the chip AUX supply	See section 3.12

Table 1: Low Power RDFC Application Circuit Components

2 APPLICATION DESIGN PARAMETERS

Table 2 lists key low power RDFC application design parameters. It provides an indication of the performance achievable with the low power RDFC topology in general and, in particular, when using this design guide. Design parameters that are specified by the user when using this guide are shown as "User-defined".

Design Parameter	Symbol	Typical Range Achievable with Low Power RDFC	Typical Value Using this Design Guide	Comments
Input voltage	V_{IN}	115 Vac (98 to 132 Vac) 230 Vac (196 to 265 Vac)	User-defined	Application designs are specified for $\pm 15\%$ of the nominal input voltage
Nominal rated output power	P_{NOM}	1 W to 6 W	User-defined	Low power RDFC chip is rated for applications in this power range
Nominal output voltage	V_{NOM}	5 V to 24 V	User-defined	
Nominal output current	I_{NOM}	0.05 A to 1.2 A	P_{NOM} / V_{NOM}	Constrains the allowable combination of P_{NOM} and V_{NOM}
Average efficiency	η	75 % to 85 %	80 %	Low power, low output voltage applications will be less efficient
Load regulation	-	10 % to 30 % of V_{NOM}	15%	Low-leakage transformers, and high value input capacitors give better load regulation
No load power consumption	P_{STBY}	100 mW – 300 mW	150 mW	Range of no load power dissipation measured with actual designs
Output ripple (line input related)	-	3 % to 20 % of V_{NOM} peak to peak	5% (230 Vac) 10% (115 Vac)	Application-dependent. Occurs at twice the line frequency.
Output ripple (switching related)	-	1 % to 5 % of V_{NOM} peak to peak	150 mV	Application-dependent. Occurs at the switching frequency.
Load pull-up capability	-	Capable of pulling-up constant voltage, constant current, constant resistance and constant power loads	Constant resistance	High leakage transformers make it easier to pull-up constant current loads
Maximum load capacitance	C_{LOAD}	4000 μF	1000 μF	
Operating frequency of the converter	F	40 kHz to 60 kHz	50 kHz	Component value adjustments may be required to achieve the target operating frequency.
Conducted emissions EN55022 class B	-	Compliant with 3-10 dB margin	Compliant with 6 dB margin	Requires optimised transformer design for high line applications

Table 2: Low Power RDFC Application Design Parameters

3 COMPONENT SELECTION

Note: Lookup tables in this design guide may not have an exact match for a parameter value required in your target application. In such cases, look up the lowest value greater than that which applies to your design. For example, if your target nominal rated power (P_{NOM}) is 2.5 W, select 3 W in the tables.

3.1 Line Rectifier (Dbridge) Selection

The input line rectifier can be implemented with two or four discrete diodes depending on the power requirement, line frequency ripple specification, efficiency specification, cost and PCB area available for the application. Use Table 3 to select a suitable type based on the nominal rated power (P_{NOM}) of your design and the expected maximum forward current. Choose the row with the lowest value of P_{NOM} greater than the rated power of your design. The shaded grey cell indicates the components suitable for the design example in section 5 (page 21). Note: the minimum recommended repetitive reverse voltage rating (V_{RRM}) of the diodes in the bridge is 300 V for 115 Vac applications and 600 V for 230 Vac applications.

Nominal Power Rating P_{NOM} (W)	I_{IN} (mA) (at 80% efficiency)		Input Rectifier Type	
	$V_{IN} = 115$ Vac	$V_{IN} = 230$ Vac	$V_{IN} = 115$ Vac	$V_{IN} = 230$ Vac
1	9	5	1N4005	1N4007
2	18	9	1N4005	1N4007
3	27	14	1N4005	1N4007
4	36	18	1N4005	1N4007
5	45	23	1N4005	1N4007
6	54	27	1N4005	1N4007

Table 3: Input Rectifier Selection

3.2 Input Capacitance ($C_{IN} = C_{in1} + C_{in2}$) Selection

The typical low power RDFC application circuit in Figure 1 on page 1 assumes the use of two parallel input capacitors (C_{in1} and C_{in2}) to achieve the total input capacitance required (C_{IN}). The value of C_{IN} required depends on the average primary current and peak-to-peak ripple voltage at the input capacitance for a given target output ripple. The total input capacitance values (C_{IN}) in Table 4 are required for 10% and 5% line-related ripple at 115 Vac and 230 Vac respectively at an average efficiency of 80%. Note: electrolytic capacitor voltage ratings should be no less than: 200 Vdc for 115 Vac applications and 400 Vdc for 230 Vac applications. The shaded grey cell in Table 4 is the input capacitance value (C_{IN}) suitable for the design example in section 5 (page 21).

Nominal Power Rating P_{NOM} (W)	$C_{IN} = C_{in1} + C_{in2}$ (μ F)	
	$V_{IN} = 115$ Vac (10% ripple)	$V_{IN} = 230$ Vac (5% ripple)
1	5	3
2	9	6
3	14	9
4	19	11
5	24	14
6	28	17

Table 4: Input Capacitance ($C_{IN} = C_{in1} + C_{in2}$) Requirement

The input capacitance value can be scaled for different percentage line-frequency ripple requirements using the following equations:

$$C_{IN-SCALED} = C_{IN} \times 10 / \text{ripple} \quad (\text{for 115 Vac applications})$$

$$C_{IN-SCALED} = C_{IN} \times 5 / \text{ripple} \quad (\text{for 230 Vac applications})$$

Where C_{IN} is the total input capacitance from Table 4;
 ripple is the revised ripple requirement (as a % of V_{NOM})
 $C_{IN-SCALED}$ is the input capacitance scaled for a different line-frequency ripple voltage requirement;

For example, the input capacitance value for 20% line-frequency ripple in a 6 W, 115 Vac application will be

$$C_{IN-SCALED} = 28 \times 10 / 20 \quad (\text{the unscaled } C_{IN} \text{ value of } 28 \mu\text{F} \text{ is from Table 4})$$

$$\approx 14 \mu\text{F}$$

3.3 Transformer Design

Transformer design is key for achieving optimum performance in low power RDFC applications. The type, size and construction of the transformer is based on the nominal rated power output (P_{NOM}), type of load, input voltage, EMC performance, size of the power supply and BOM cost. Low power RDFC transformers have three functional windings: primary, secondary and auxiliary.

3.3.1 Core Size Selection

Table 5 gives recommended sizes for typical applications based on nominal rated power and input voltage. The recommendations assume use of low-loss core material suitable for 50 kHz operation, e.g. PC40. The shaded grey cell in Table 5 contains the core type recommended for the design example on page 21.

Nominal Power Rating P_{NOM} (W)	Recommended Core size	
	$V_{IN} = 115 \text{ Vac}$	$V_{IN} = 230 \text{ Vac}$
1	EE13	EE13
2	EE13	EE13
3	EE13	EE13
4	EE13	EE16
5	EE13	EE16
6	EE13	EE16

Table 5: Core Size Selection Table

3.3.2 Number of Secondary Turns (N_S)

Table 6 gives the fractional number of secondary turns (N_{SPV}) required per volt on the anode of the output diode (Dout). The actual number of secondary turns (N_S) required is given by $N_S = N_{SPV} \times (V_{NOM} + V_{DOUT})$, where V_{DOUT} is the nominal voltage drop across Dout. The shaded grey cell is value of N_{SPV} for the design example on page 21.

Core Size	EE13	EE16
N_{SPV}	1.52	1.35

Table 6: Fractional Number of Secondary Turns Required per Output Volt (N_{SPV})

Note: N_S must be rounded up to the nearest whole number. For example, in a 115 Vac, 6 W, 9 V application, recommended core is E13 (from Table 5) so the number of secondary turns per output volt (from Table 6) is 1.52. The actual number of secondary turns to use is then given by:

$$N_S = N_{SPV} \times (V_{NOM} + V_{DOUT})$$

$$N_S = 1.52 \times (9 + 0.5) = 14.44 \quad (\text{assuming } V_{DOUT} \approx 0.5 \text{ V})$$

$$N_S = 15 \quad (\text{rounded up to nearest whole number})$$

Rounding up the number of secondary turns means that the number of turns on the primary and secondary windings must be scaled up in order to preserve the correct turns ratio. The simple calculation is explained in the following sections.

3.3.3 Number of Primary Turns (N_P)

The typical number of primary turns N_{PTYP} for a given input voltage (V_{IN}) and core size is shown in Table 7. These numbers are consistent with fully resonant operation, core flux swing from -60% to 100%, maximum flux density (B_{MAX}) of 300 mT, maximum input voltage and 10% design margin. The shaded grey cell is the typical number of primary turns for the design example on page 21.

Core Size	EE13	EE16
V_{IN} 115 Vac	214	N/A
V_{IN} 230 Vac	431	384

Table 7: Typical Number of Primary Turns (N_{PTYP})

To maintain the correct turns ratio the number of primary turns must be scaled to account for the amount by which the number of secondary turns was rounded up (see section 3.3.2):

$$N_P = N_{PTYP} \times N_S (\text{after rounding}) / N_S (\text{before rounding})$$

For example, in a 115 Vac, 6 W, 9 V application, N_P from Table 7 is 214. Using the rounded and unrounded number of secondary turns for that application (see section 3.3.2) the required number of primary turns is:

$$N_P = 214 \times 15 / 14.44$$

$$N_P = 223 \quad (\text{rounded up to nearest whole number})$$

3.3.4 Number of Auxiliary Turns (N_{AUX})

The minimum number of auxiliary turns (N_{AUXMIN}) required for a given core size is shown in Table 8. The shaded grey cell is the number to choose for the design example in section 5 (page 21).

Core Size	EE13	EE16
N_{AUXMIN}	12	11

Table 8: Minimum Number of Auxiliary Turns (N_{AUXMIN})

To maintain the correct turns ratio the number of auxiliary turns must be scaled (just like the number of primary turns) to account for the amount by which the number of secondary turns was rounded up (in section 3.3.2):

$$N_{AUX} = N_{AUXMIN} \times N_S (\text{after rounding}) / N_S (\text{before rounding})$$

In the 115 Vac, 6 W, 9 V application, N_{AUXMIN} from Table 8 is 12. Using the rounded and unrounded number of secondary turns for that application (see section 3.3.2) the required number of auxiliary turns is:

$$N_{AUX} = 12 \times 15 / 14.44$$

$$N_{AUX} = 13 \quad (\text{rounded up to nearest whole number})$$

3.3.5 Secondary Winding Conductor Size

Use Table 9 to select a suitable conductor size for the secondary winding wire. Note that for some combinations of core size and output voltage the windings must be multilayer. The shaded grey cell contains the conductor size selected for the design example in section 5 (page 21).

Core Size	Nominal Output Voltage V_{NOM} (Vdc)								
	5	6	7.5	9	12	15	18	21	24
EE13	0.4	0.3	0.2	0.2M	0.2M	0.2M	0.2M	0.2M	0.2M
EE16	0.6	0.45	0.35	0.25	0.2M	0.2M	0.2M	0.2M	0.2M

Table 9: Secondary Wire Conductor Diameter (mm) M = Multilayer

3.3.6 Primary Winding Conductor Size

Use Table 10 to select a suitable conductor size for the primary winding wire, based on nominal rated power and input voltage. The shaded grey cell contains the conductor size selected for the design example in section 5 (page 21).

Nominal Power Rating P_{NOM} (W)	$V_{IN} = 115$ Vac	$V_{IN} = 230$ Vac
1	0.15	0.1
2	0.15	0.1
3	0.15	0.1
4	0.15	0.1
5	0.15	0.1
6	0.15	0.1

Table 10: Primary Winding Wire Conductor Diameter (mm)

3.3.7 Transformer Inductances

The transformer primary inductance (measured at 50 kHz with the secondary and auxiliary windings open circuit) should be approximately as shown in Table 11.

Core Size	EE13	EE16
$V_{IN} = 115$ Vac	52	N/A
$V_{IN} = 230$ Vac	37**	54**

Table 11: Typical Primary Winding Inductance (mH)

** Gapped cores are required for 230 Vac applications to avoid core saturation. EE13 cores should be gapped to give an effective AL value of 200 nHN² and EE16 cores should be gapped to give an effective AL value of 365 nHN².

Typical leakage inductance values are around 400 μ H for 115 Vac applications and around 1 mH for 230 Vac applications. Measure leakage inductance with the secondary and auxiliary windings shorted.

3.3.8 Transformer Construction

Figure 2 shows the construction of a typical, low-leakage inductance RDFC transformer. The auxiliary winding provides power to the controller IC during normal operation. A screen is placed between the primary and secondary to minimise noise coupling.

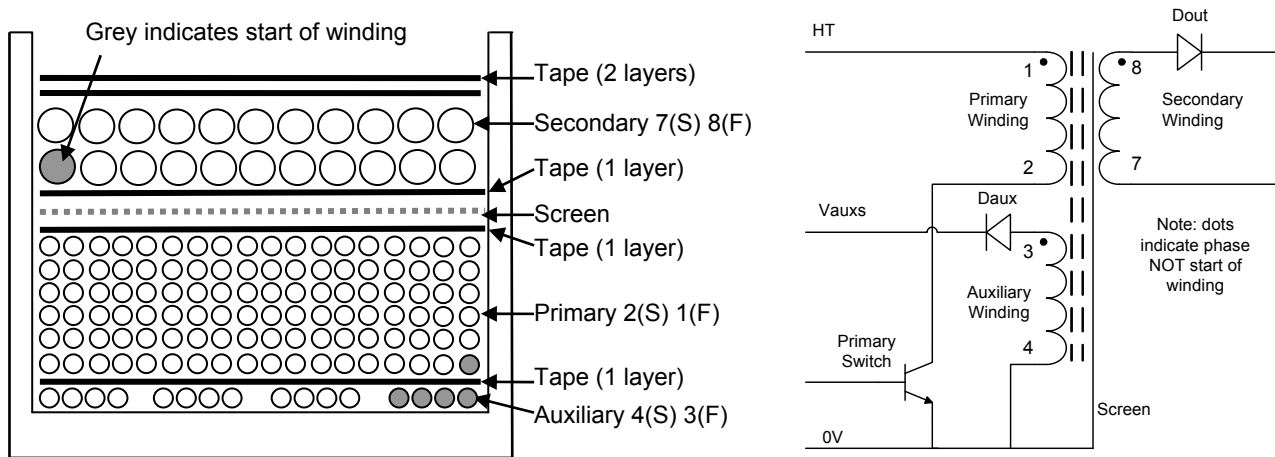


Figure 2: Transformer Cross Section and Schematic
 Note: s(S) means start on pin s, f(F) means finish on pin f

Transformer construction can be varied to meet EMC targets and optimise leakage inductance according to particular application requirements. Table 12 summarises winding instructions.

Winding	Wire	Layers	Comments
Auxiliary	Grade 2 enamelled copper wire. 0.15 mm diameter conductor.	1	Full width neatly wound. Use optimum number of multi-filar windings to cover the bobbin width. After termination to the pins, put a small piece of tape on the inside of the bobbin, covering the winding lead-outs.
Tape	Class B Polyester film	1	Full width with a small overlap at the ends.
Primary	Grade 2 enamelled copper wire. Refer to Table 10 for conductor diameter.	Multiple	Full width neatly wound layers. After termination to the pins, put a small piece of tape on the inside of the bobbin covering the winding lead-outs.
Tape	Class B polyester film	1	Full width with a small overlap at the ends.
Screen	Copper foil or grade 2 enamelled copper wire.	1	Cover the full width of the bobbin. Connect to 0 V (pin 4) of the bobbin (see Figure 2). A method for implementation of wound screens is described in the patent JP60226112 (Hitachi Ltd, Nippon Telegraph and Telephone, 1985)
Tape	Class B polyester film	1	Full width with a small overlap at the ends.
Secondary	Triple insulated wire (Furukawa TEX-E). Refer to Table 9 for conductor diameter.	Multiple	Use flying leads with E13 or E16 cores. Start at the top of the bobbin, against the wall on the side near to the secondary side of the PCB. Mark the start with a sleeve. Avoid placing the wire hard up against the wall on the primary side of the PCB.
Tape	Class B polyester film	2	Full width with a small overlap at the ends.

Table 12: Winding a Low-leakage Transformer for a Typical Low Power RDFC Application

Note also:

- Care should be taken to avoid crossing the start and finish ends of windings near the pins;
- Minimise the separation between primary and secondary in order to achieve low-leakage inductance;
- Secure the cores with glue or tape so that the faces are in firm contact;
- Wrap the core with three complete layers of polyester tape wider than the core;
- Varnish-dip or vacuum impregnate. Avoid getting varnish on the pins.

3.4 Output Capacitor (Cout)

The output capacitor (Cout) is selected according to requirements for ripple current rating, effective series resistance (ESR), size and cost. Table 13 shows the minimum ripple current rating and maximum ESR for Cout for a given nominal output current (I_{NOM}), assuming a low leakage transformer design and peak-to-peak switching ripple voltage of 150 mV. The shaded grey cells are the ratings chosen for the design example in section 5 (page 21).

$I_{NOM} = P_{NOM} / V_{NOM}$ (A)	Ripple Current (A rms)	ESR Max (mΩ)
0.05	0.06	857
0.1	0.11	429
0.2	0.22	214
0.4	0.45	107
0.5	0.56	86
0.6	0.67	71
0.8	0.89	54
1	1.12	43
1.2	1.34	36

Table 13: Output Capacitor (Cout) Rating

The recommended minimum dc voltage rating for Cout is $1.25 \times V_{NOM}$.

3.5 Primary Switch Transistor (Q1)

Selection of the primary switch transistor (Q1) should take into account the following factors:

- The maximum collector voltage (V_{CE}) it must withstand under all possible operating conditions;
- The maximum collector current (I_C) before over current protection (OCP) comes into effect;
- The worst case voltage and current stress it has to withstand during turn off;
- The minimum h_{FE} required, which is determined by the base drive capability of the low power RDFC controller.

Table 14 lists transistor types suitable for use as the primary switch in low power RDFC applications. The shaded grey cells indicate the type chosen for the design example in section 5 (page 21).

Nominal Power Rating P_{NOM} (W)	$V_{IN} = 115$ Vac		$V_{IN} = 230$ Vac	
	Q1 Type	Package	Q1 Type	Package
1	MJE13003/TS13003	TO-92	KSC5042M	TO-126
2	MJE13003/TS13003	TO-92	KSC5042M	TO-126
3	MJE13003/TS13003	TO-92	KSC5042M	TO-126
4	MJE13003/TS13003	TO-92	TT2274A	TO-126
5	TS13003	TO-92	TT2274A	TO-126
6	TS13003	TO-92	TT2274A	TO-126

Table 14: Transistor Types Suitable for Use as the Primary Switch (Q1)

Voltage rating requirements of the primary switch are:

230 Vac operation: $V_{cbo} \geq 1400$ V, $V_{ceo} \geq 700$ V

115 Vac operation: $V_{cbo} \geq 700$ V, $V_{ceo} \geq 400$ V

BJTs with high hFE rating is required for 115 Vac applications above 4 W.

Manufacturers' datasheets should be consulted to ensure that particular component chosen for Q1 meets these specifications.

3.6 Resonant Capacitor (Ccol) and Cp Capacitor Selection

The resonant capacitor (Ccol) is situated between the primary switch collector and the low power RDFC controller COL pin. Table 15 gives the recommended values of Ccol for different core types assuming 50 kHz operating frequency, the number of primary turns specified in Table 7, a screen between primary and secondary and PC40 core material. When selecting Ccol, avoid dielectric material with ageing characteristics and high dielectric absorption with applied voltage or temperature. **Class 1 ceramic material such as C0G (NP0) is strongly recommended.** Ccol must be a high voltage type: 1 kVdc for 115 Vac applications and 1.5 kVdc for 230 Vac applications. The shaded grey cell in Table 15 indicates the value chosen for the design example in section 5 (page 21).

Core Size	Ccol (pF)	
	$V_{IN} = 115$ Vac	$V_{IN} = 230$ Vac
E13	47	47
E16	N/A	47

Table 15: Resonant Capacitor (Ccol) Value

Cp takes the same value as Ccol but only needs a dc rating of 50 V.

3.7 Output Diode (Dout) Selection

The output diode (Dout) must withstand continuous operation under overload conditions and reverse voltage at peak input voltage. For efficiency reasons, Schottky diodes should be used for output voltages (V_{NOM}) up to 12 V. Above that level fast epitaxial diodes are suitable. In Table 16 V_{RRMIN} is the minimum recommended reverse voltage rating (V_{RRM}) for Dout and $I_{F(AV)}$ is the minimum recommended average forward current handling capability. Select an output diode from Table 16 based on application rated output current (I_{NOM}) and output voltage (V_{NOM}). Where no diode type is recommended it is because the design rating is outside the range that can be created using this guide. The shaded grey cell indicates the diode type chosen for the design example in section 5 (page 21).

$I_{NOM} = P_{NOM} / V_{NOM}$ V_{NOM} (A)	$I_{F(AV)}$ (A)	Application Nominal Output Voltage (V_{NOM})								
		5 V	6 V	7.5 V	9 V	12 V	15 V	18 V	21 V	24 V
0.05	0.06	-	-	-	-	-	-	-	SF14G	SF14G
0.1	0.13	-	-	-	-	1N4148	1N4148	SR110	SF14G	SF14G
0.2	0.25	1N5818	1N5819	1N5819	SB160	SB160	SR110	SR110	SF14G	SF14G
0.4	0.50	1N5818	1N5819	1N5819	SB160	SB160	SR110	-	-	-
0.5	0.63	1N5818	1N5819	1N5819	SB160	SB160	-	-	-	-
0.6	0.75	1N5818	1N5819	1N5819	SB160	-	-	-	-	-
0.8	1.00	1N5822	1N5822	1N5822	-	-	-	-	-	-
1	1.25	1N5822	1N5822	-	-	-	-	-	-	-
1.2	1.50	1N5822	-	-	-	-	-	-	-	-
Dout V_{RRMIN} rating		26 V	30 V	38 V	45 V	59 V	73 V	88 V	102 V	116 V

Table 16: Output Diode (D_{OUT}) Selection

3.8 COL Pin Protection (R_{col})

Diodes Dcol1, Dcol2 and resistor Rcol protect the controller COL pin from voltage and current excursions. 1N4148 or any other fast recovery diode with at least 0.2A forward current capability is suitable for Dcol1 and Dcol2. The value of Rcol should be 100 Ω .

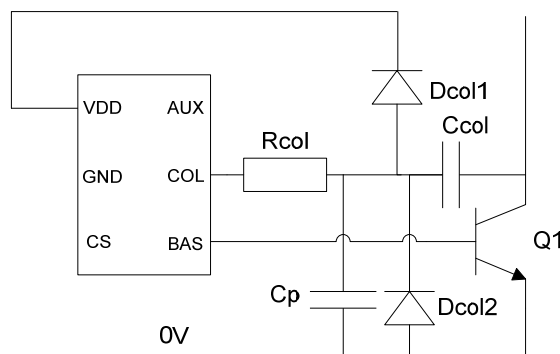


Figure 3: COL pin protection circuit

3.9 Current Sense Resistors (R2 and Rcs)

The low power RDFC controller has two internal threshold values called OCPH (overcurrent protection high) and OCPL (overcurrent protection low) which are set by two external resistors, R2 and Rcs (see Figure 4). OCPH sets the point at which the controller will go into Foldback mode (overload protection). OCPL is used to optimise switching duty cycle for converter efficiency at low loads. Refer to the low power RDFC controller datasheet (DS-1639) for further information.

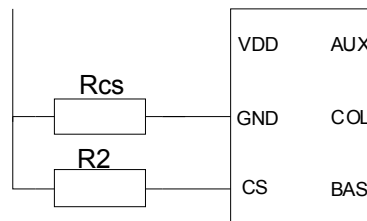


Figure 4: OCPH and OCPL Programming Circuit

The value of R2 is typically 470 Ω but can be adjusted to suit a particular application (see section 4.7). Table 17 gives recommended Rcs values and power ratings for given mains input voltage (V_{IN}) and nominal rated power (P_{NOM}). The shaded grey cell indicates the value and power rating of Rcs chosen for the design example in section 5 (page 21).

Nominal Power Rating P_{NOM} (W)	115 Vac		230 Vac	
	Ω	W	Ω	W
1	6.47	0.125	12.90	0.125
2	3.23	0.125	6.45	0.125
3	2.16	0.125	4.30	0.125
4	1.62	0.125	3.22	0.125
5	1.29	0.125	2.58	0.125
6	1.08	0.125	2.15	0.125

Table 17: Rcs Resistor Selection

3.10 AUX Pin Supply Resistor (Raux)

Base drive current for the primary switch (Q1) is supplied via the AUX pin of the controller. Table 18 gives recommended values of Raux according to application nominal rated power (P_{NOM}). The shaded grey cell indicates the value of Raux for the design example in section 5 (page 21).

Nominal Power Rating P_{NOM} (W)	Raux (Ω)	
	115 Vac	230 Vac
1	47	22
2	47	22
3	47	22
4	47	22
5	47	22
6	47	22

Table 18: Raux Resistor Value Selection

3.11 V_{DD} Feed Resistor (R_{dd})

A V_{DD} feed resistor is required that will provide sufficient supply current to the chip (via the VDD pin) at minimum auxiliary winding voltage (about 6 V) but which dissipates minimum power itself (to limit design no load power). For applications up to 6 W a value of 330 Ω should be sufficient.

3.12 Other Components

Refer to Table 19 for selection of components not covered in preceding sections.

Component	Description	Notes
Lfilt	Input filter inductor	Reduces differential mode EMI. Typically 1 mH.
Fuse	Antisurge fuse	Provides protection in the event of failure in the converter circuit.
Rfuse	Flameproof fusible Resistor	Also limits inrush current and assists with surge immunity. Typically 22 Ω .
Rht	VDD supply resistor	Must meet operating voltage and fail safely in case of component failures. Typically two SMT resistors or two flameproof metal oxide leaded resistors (in series to share voltage stress). $V_{IN} = 115 \text{ Vac}$: Rht1 = Rht2 = 2.7 M Ω total resistance 5.4 M Ω $V_{IN} = 230 \text{ Vac}$: Rht1 = Rht2 = 4.7 M Ω total resistance 9.4 M Ω
Csnub	Snubber to reduce EMI from output diode turn-off	A ceramic type, with value typically between 1 nF and 2.2 nF. Voltage rating should be at least equal to the V_{RRM} rating of Dout (see Table 16 in section 3.7). Value may need to be optimised to meet EMC emission limits.
Rsnub	Snubber to reduce EMI from output diode turn-off	Typically 10 Ω to 100 Ω . Value may need to be optimised to meet EMC emission limits.
Rout	Output bleed resistor	To limit voltage rise with no load and provide a discharge path when V_{IN} is disconnected. Rout is typically only used in applications requiring tight output regulation from no load to full load. Choose a value of, say, 1 k Ω /V output. I.e. Rout (k Ω) = V_{NOM} .
Cdd	VDD decoupling capacitor	Decouples the chip VDD supply. A 1 μ F, 16 V ceramic type is suitable for use as Cdd.
Daux	Auxiliary voltage rectifier	1N4148 is a suitable fast recovery diode for use as Daux.
Caux	AUX decoupling capacitor	Decouples the chip AUX supply rail. A 470 nF, 16 V ceramic type is suitable for use as Caux.

Table 19: Selection of Other Components

4 TESTING AND TROUBLESHOOTING YOUR DESIGN

Once the components are selected and the transformer constructed a prototype of the design can be made. This section takes you through a stepwise approach to testing and observing behaviour of your application design. Refer to the low power RDFC controller datasheet (reference DS-1639) for further information about the ICs and their operating modes.

4.1 Safety

Offline power supplies, particularly in a development situation, can present hazards including, but not limited to, electric shock, high temperatures, fire and smoke. They should be operated and used only by competent, trained personnel. In particular:

- The unit to be tested should be checked for design and build errors before applying mains power;
- The unit under test should be powered via a suitable isolating transformer and a variac;
- Hazardous voltages are present in both normal and abnormal operating conditions;
- Insulation between high voltage and low voltage parts may not provide safety isolation;
- All connections should be regarded as LIVE and HAZARDOUS.

4.2 Typical Low Power RDFC IV Characteristic

Figure 5 shows a typical low power RDFC IV characteristic for designs made with this guide. It is labelled with the names of the various controller operating modes. The following sections describe these modes in more detail with oscilloscope screen images of the primary switch collector voltage that is expected in each.

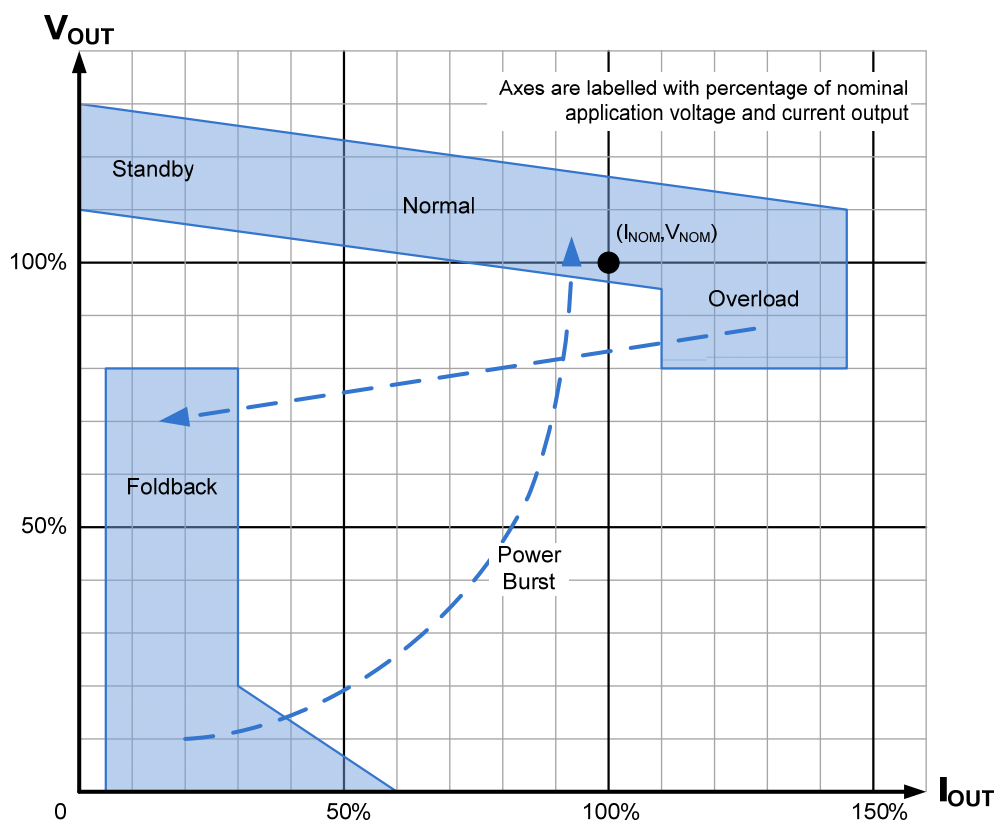


Figure 5: Typical Low Power RDFC Power Supply Characteristic Indicating Different Active Modes of Operation

4.3 First Power-up (No Load) – Standby Mode

Please read the safety advice in section 4.1 before applying power to any application circuit.

Attach a high voltage oscilloscope probe to the collector of the primary switch (Q1). Apply nominal input voltage (115 Vac or 230 Vac) with no load on the output. Observe the collector voltage waveform. It should be similar to the oscilloscope plot in Figure 6 (note, in Figure 6 $V_{IN} = 115 \text{ Vac}$).

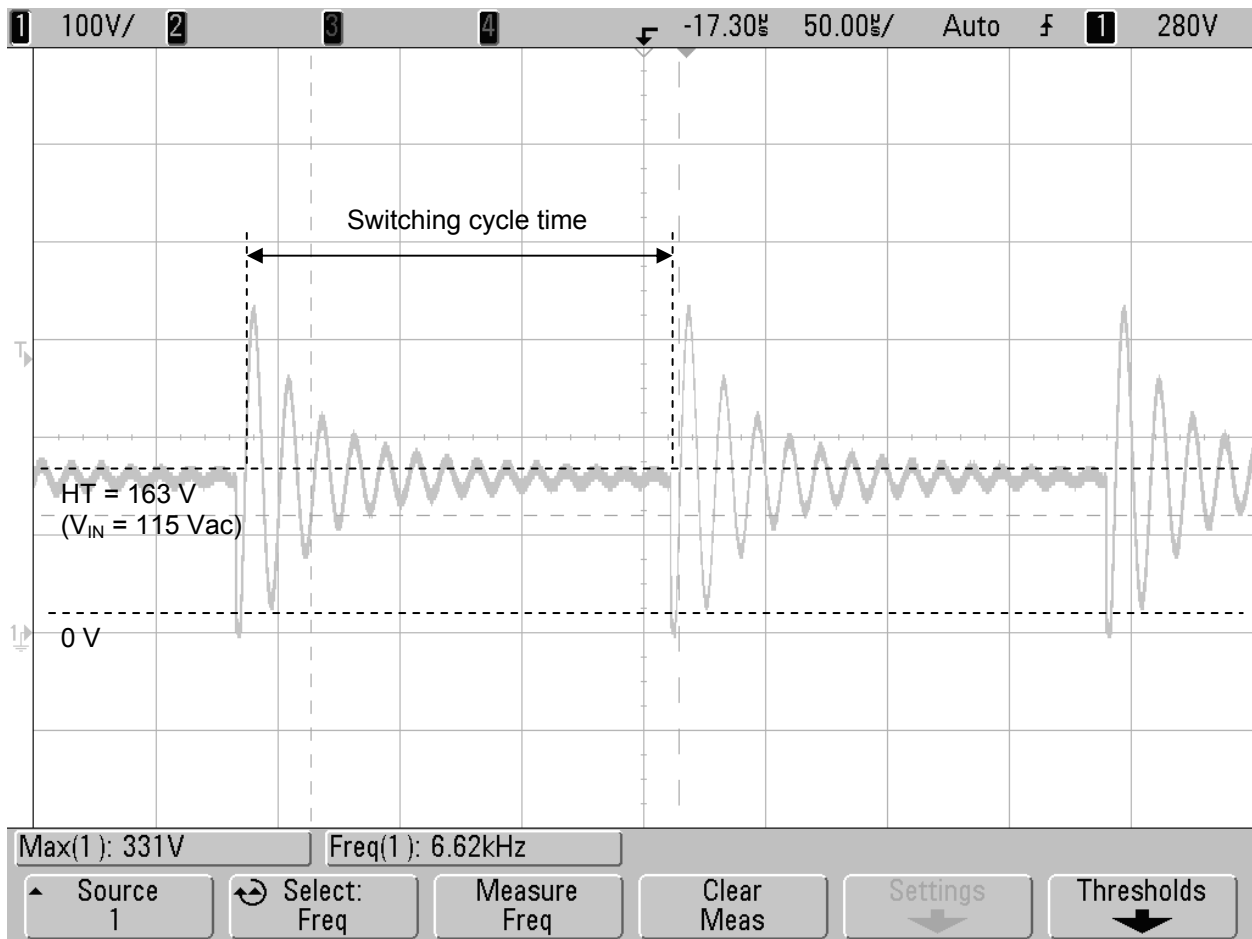


Figure 6: Q1 Collector Voltage Waveform With No Load (Controller in Standby Mode)

- If no switching signal is observed check the primary side components for connectivity and correct polarity;
- If there are only a few switching cycles, say every approximately 10 ms, check the components connected to the auxiliary winding;
- If the switching cycle time of the observed signal (dominated by the Q1 off-time) is below 150 μs , increase the value of R2 in 10% steps until the period is approximately 200 μs . This reduces no load power consumption.

4.4 Running with P_{OUT} at About 25% of Rated Power

Still with nominal input voltage, attach a 25% load to observe an oscilloscope plot similar to the one in Figure 7. It shows the converter changing between Standby and Normal modes – this is expected low power RDFC behaviour with the load at around 25% of the application rated power. If only Normal mode operation is observed with no changes in and out of Standby (i.e. fully resonant switching and no change in the on-time of switching cycles), increase the value of R2 (in steps of, say, 10%) until the expected waveform is observed. If only Standby operation is observed with no change to Normal mode, try reducing the value of R2, again in 10% steps.

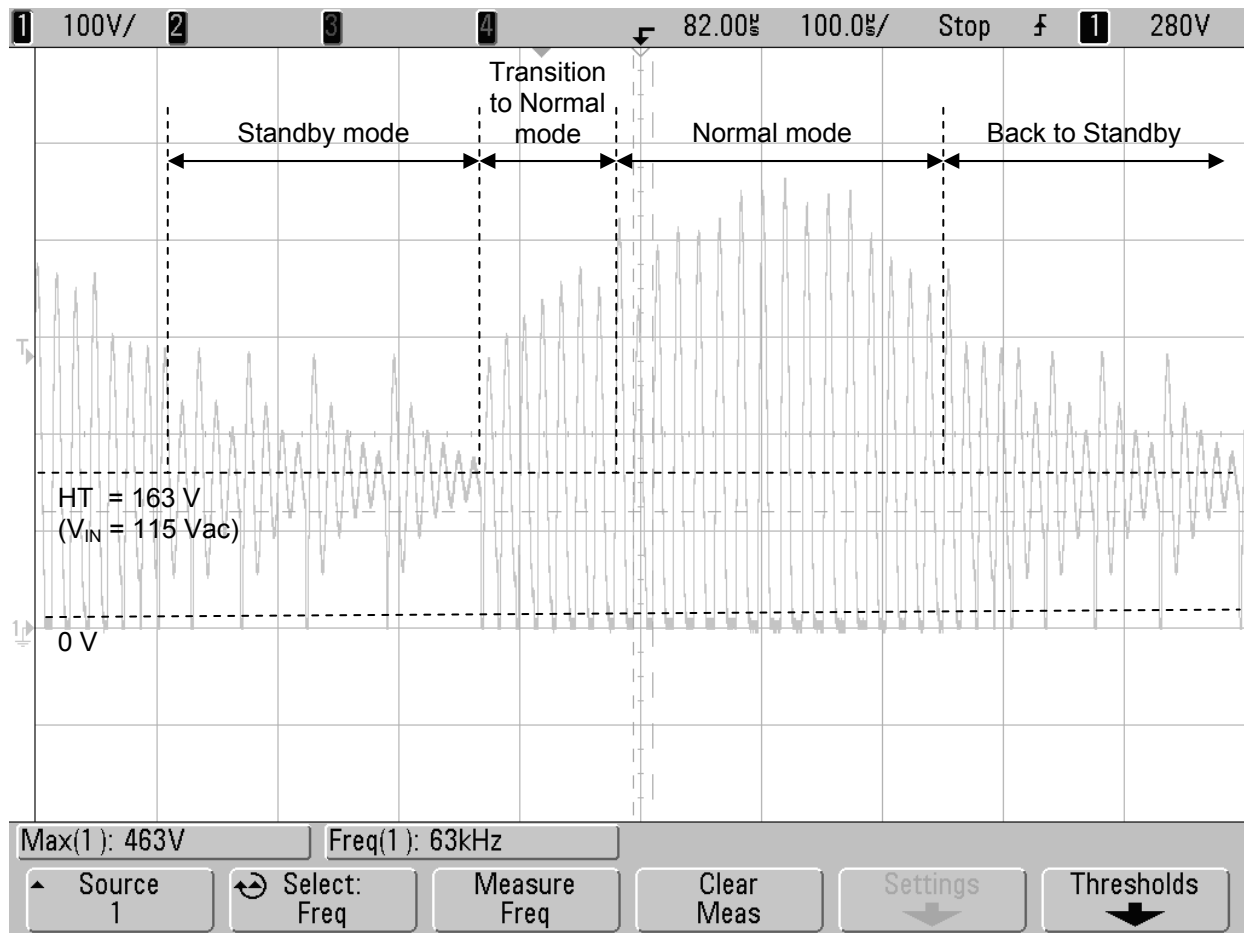


Figure 7: Q1 Collector Voltage Waveform with P_{OUT} at about 25% of Rated Power with Expected Transitions Between Low Power RDFC Controller Operating Modes Standby and Normal

4.5 P_{OUT} Up to Rated Power – Continuous Normal Mode

Increase the load to about 60% of rated power, at nominal input voltage, to observe continuous operation in Normal mode. The oscilloscope display should be similar to that shown in Figure 8. An operating frequency of 40 kHz to 60 kHz is typical for low power RDFC designs. It can be adjusted by changing the value of the C_{col} capacitor. Increasing C_{col} will make the operating frequency lower, decreasing C_{col} will make it higher. If you need to adjust the operating frequency, try changing C_{col} in steps of about 10% of the nominal value used.

Continuous Normal mode operation should be observed above when P_{OUT} is above about 40% of nominal rated power (P_{NOM}). If you are still seeing transitions between Standby and Normal modes (like those in Figure 7) at or above 40% of rated power your design may emit audio noise. You can adjust the load threshold above which Normal-only mode operation occurs by changing the value of R2. Decreasing the value of R2 will lower the threshold to a lower power level, increasing the value of R2 will raise the threshold. If you need to change R2, try steps of 10%.

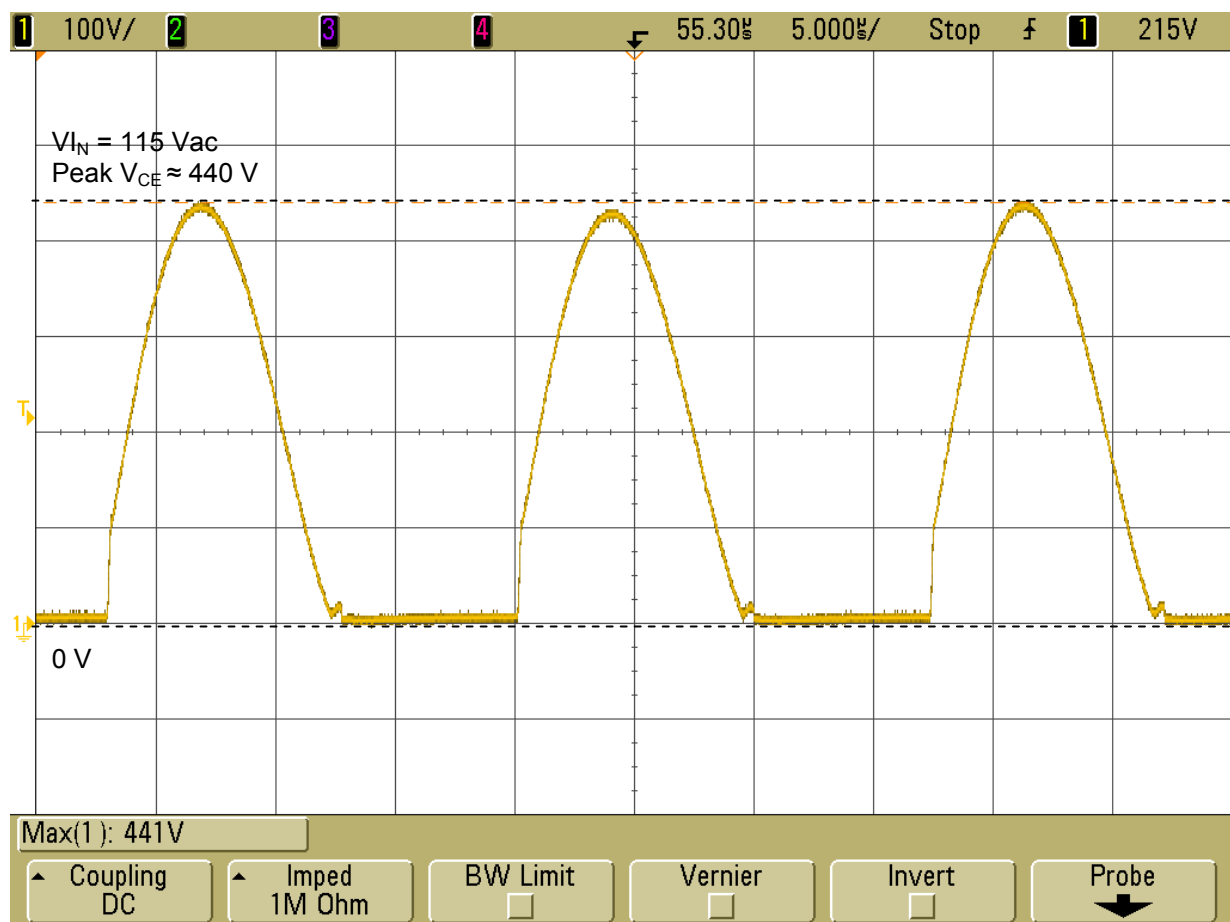


Figure 8: Q1 Collector Voltage Waveform with P_{OUT} Approaching Rated Power (P_{NOM})
(Normal Mode – Continuous Resonant Switching)

4.6 P_{OUT} Above Rated Power - Overload Mode

If you increase the load towards 100% of the rated power and beyond, the Q1 collector voltage waveform will become like that in Figure 9. Note the steep rise in the collector voltage before the start of the more sinusoidal shape seen in Normal mode (Figure 8).

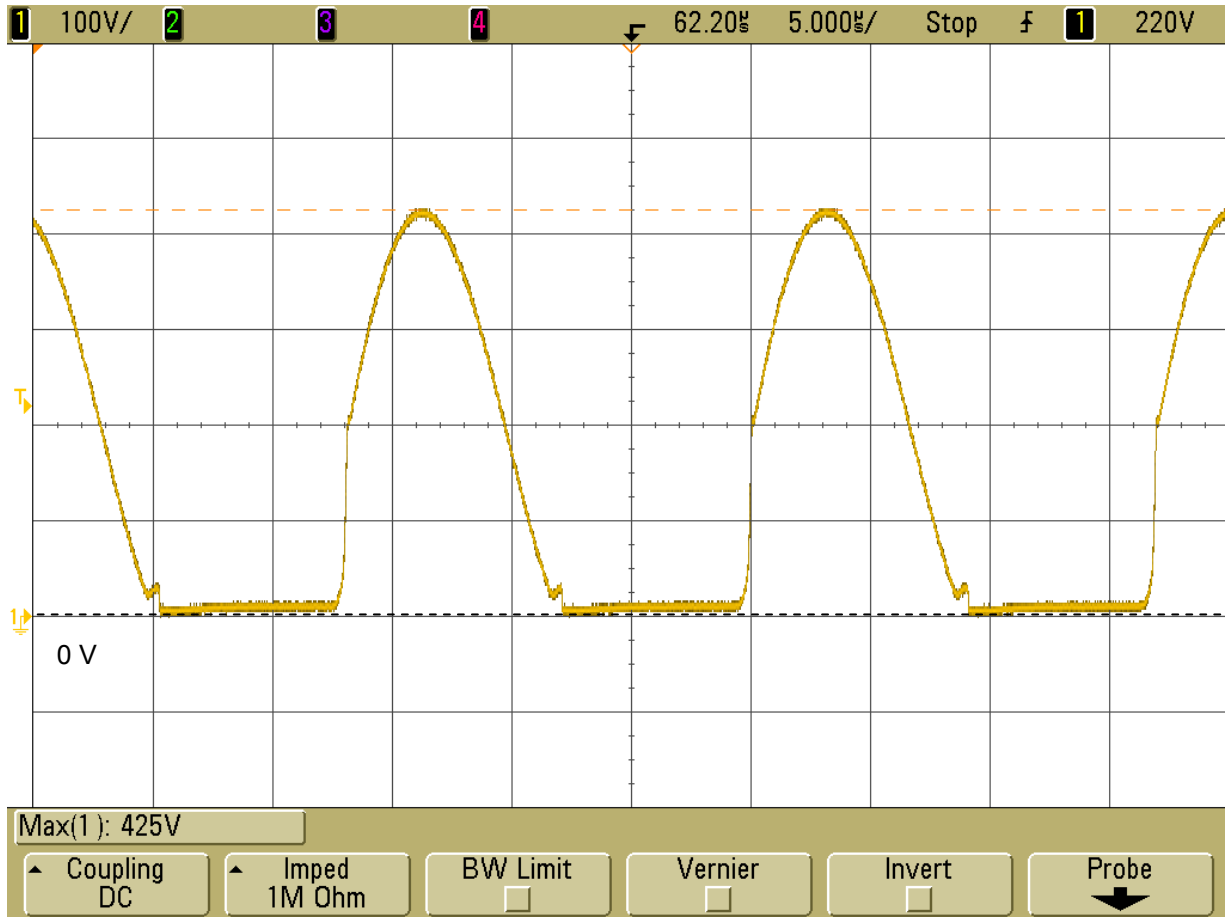


Figure 9: Q1 Collector Voltage Waveform at Rated Load and Above (Overload Mode)

4.7 Short Circuit Load - Foldback Mode

Increasing the load beyond about 130% of nominal rated power (P_{NOM}) will make the low power RDFC controller start alternating between Foldback and Power Burst modes of operation. The Q1 collector voltage waveform should be like that in Figure 10. Foldback mode with its low duty cycle switching keeps the converter running (powered from the auxiliary winding) with low power dissipation in the application circuit and the load. The higher duty cycle switching in Power Burst mode is there to initiate resumption of Normal mode power conversion when the overload (short circuit) condition is removed.

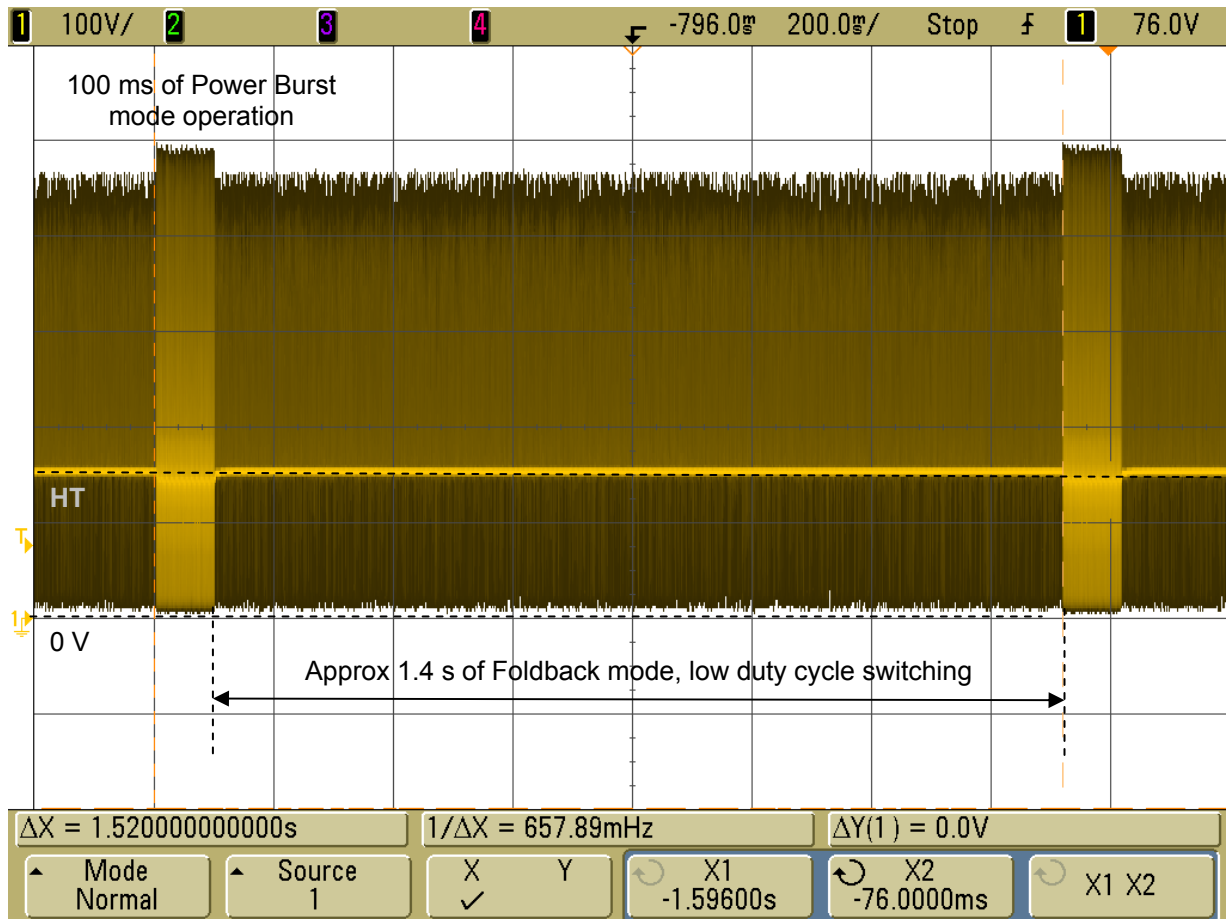


Figure 10: Q1 Collector Voltage Waveform in Foldback Mode

- You can adjust the load level at which the converter goes in to Foldback by changing the value of the Rcs resistor. To raise the threshold (i.e. enter Foldback at a higher load), decrease the value of Rcs. To lower the threshold (i.e. enter Foldback at a lower load), increase the value of Rcs.
- If the threshold at which your design enters Foldback mode is much too low the converter may fail to return to Normal mode when the short circuit condition is removed. If you experience this, raise the threshold at which the converter goes into Foldback (as described above). Alternatively, you can increase the transformer leakage inductance, which will make the transition from Overload to Foldback mode occur at a lower voltage.

5 EXAMPLE APPLICATION DESIGN

5.1 Application Design Parameters

Table 20 is the target specification for a design example made using this guide.

Parameter	Application Requirement
Input voltage (V_{IN})	115 Vac \pm 15%
Rated output power (P_{NOM})	3 W
Nominal output voltage (V_{NOM})	6 V at nominal mains input and $P_{OUT} = P_{NOM}$
Nominal output current (I_{NOM})	0.5 A (= $P_{NOM} / V_{NOM} = 3 / 6 = 0.5$ A)
Average efficiency (η)	> 75 %
Load regulation	< 20% of V_{NOM}
No load power consumption (P_{STBY})	< 150 mW
Output line ripple	< 600 mV (10% of V_{NOM}) at twice line-frequency
Output switching ripple	< 150 mV (2.5% V_{NOM})
Load pull-up capability	Constant resistance with max C_{LOAD}
Maximum load capacitance (max C_{LOAD})	1000 μ F
Operating Frequency	Typically 50 kHz
Overcurrent protection	Transition to Foldback mode occurs between I_{NOM} and 1.5 x I_{NOM}
Emissions	EN55022 class B with 6dB pass margin
Input power (P_{IN}) with short circuit load	< 2 W
Turn-on delay	< 500 ms

Table 20: Specification for the Design Example

5.2 Components Selected Using The Design Guide

Table 21 summarises the components in the design example which were determined using this guide.

Component		Guide Type/Value/Rating	Refer to Section	Actual Type/Value/Rating
Low Power RDFC controller IC		C2471LX2 (SOT23-6)	-	C2471LX2 (SOT23-6)
Dbridge		1N4005	Section 3.1, page 5	1N4005, 1 A, 600 V
$C_{IN} = C_{in1} + C_{in2}$		14 μ F	Section 3.2, page 5	10 μ F, 4.7 μ F (200 V)
Lfilt		1 mH	Table 19, page 14	1 mH
Transformer core		EE13	Section 3.3.1, page 6	EE13-PC40
Bobbin		n/a	n/a	
Secondary turns N_S		9.88 rounded to 10	Section 3.3.2, page 6	10
Primary turns N_P		214 scaled to 217	Section 3.3.3, page 7	217 (= 214 x 10 / 9.88 rounded)
Auxiliary turns N_{AUX}		13	Section 3.3.4, page 7	13 (= 12 x 10 / 9.88 rounded)
Secondary conductor		0.3 mm	Section 3.3.5, page 8	0.3 mm
Primary conductor		0.15 mm	Section 3.3.6, page 8	0.15 mm
Auxiliary conductor		0.15 mm	Table 12, page 9	0.15 mm
Primary inductance		52 mH	Section 3.3.7, page 8	55 mH
Leakage inductance		400 μ H	Section 3.3.7, page 8	313 μ H
Output capacitor Cout	I_{RMS}	0.56 A	Section 3.4, page 10	10ZL470M8X11.5, 470 μ F, 10 V dc, ripple rating 0.76 A, ESR 72 m Ω
	ESR	86 m Ω		
Primary switch Q1		MJE13003	Section 3.5, page 10	MJE13003, 1.5 A, 700 V, TO-92
Resonant capacitor C_{COL}		100 pF	Section 3.6, page 11	47 pF, 1 kV rated
Programming capacitor C_p				47 pF, 50 V
Output diode Dout	$I_{F(AV)}$	0.63 A	Section 3.7, page 12	1N5819, 1 A, 40 V
	V_{RRM}	30 V		
Dcol1 and Dcol2		1N4148	Section 3.8, page 12	1N4148, 200 mA, 75 V
Rcol		100 Ω		100 Ω , 0.125 W
Rcs		2.16 Ω	Section 3.9, page 13	3.3 Ω // 3.3 Ω , 0.125 W
R2		470 Ω		470 Ω , 0.125 W
Raux		47 Ω	Section 3.10, page 13	47 Ω
Rdd		330 Ω	Section 3.10, page 13	330 Ω
Fuse		-	Table 19, page 14	0.5 A, 125Vac antisurge type
Rfuse		22 Ω	Table 19, page 14	Not fitted
Rht1, Rht2		Both 2.7 M Ω	Table 19, page 14	Both 2.7 M Ω , 250 Vdc
Csnub		1 nF to 2.2 nF	Table 19, page 14	1 nF, 50 V
Rsnub		10 Ω to 100 Ω	Table 19, page 14	10 Ω
Rout (optional)		6 k Ω	Table 19, page 14	Not fitted
Cdd		1 μ F	Table 19, page 14	1 μ F, 50 V
Daux		1N4148	Table 19, page 14	1N4148
Caux		470 nF	Table 19, page 14	470 nF

Table 21: Components in the Design Example Selected Using This Guide

5.3 Measured Performance

Table 22 summarises the results achieved when measuring a unit of the example design. Unless otherwise stated the operating conditions are:

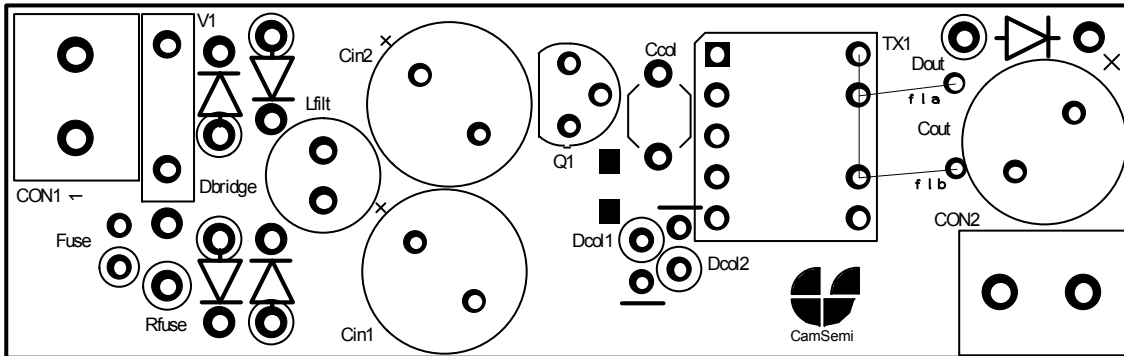
- $V_{IN} = 115 \text{ Vac}$
- Power in to the load $P_{OUT} = P_{NOM}$ (rated power)
- Resistive load (load capacitance $C_{LOAD} = 0$)

Parameter	Application Requirement	Achieved Performance	Conditions
Nominal output voltage V_{NOM}	6 V	6.35 V	Nominal mains input (V_{IN}) Delivering rated power (P_{NOM})
Average efficiency	> 75%	75.9 %	Average of efficiency at 4 load points: 25%, 50%, 75%, 100% of rated P_{NOM}
Load regulation	< 20%	15.2 %	Load from 10 mA to I_{NOM}
No load power (P_{STBY})	< 150 mW	112 mW	
Output line ripple	900 mV pk-pk at twice line frequency	470 mV pk-pk	
Output switching ripple	150 mV pk-pk at switching frequency	112 mV pk-pk	
Load pull up capability	Constant resistance	OK. See section 5.9.	$C_{LOAD} = 1000 \mu\text{F}$
Operating frequency	Typically 50 kHz	44.2 kHz	
Overcurrent protection	Transition to Foldback mode occurs between $1.3 \times I_{NOM}$ and $1.5 \times I_{NOM}$	Transition at $\approx 1.5 \times I_{NOM}$	
Emissions	EN55022 class B	OK. See section 5.15.	
Short circuit P_{IN}	< 2 W	0.8 W	
Load transient response	Stable operation. Output should remain within max-min regulation.	OK. See sections 5.11 and 5.12	$C_{LOAD} = 1000 \mu\text{F}$
Turn-on delay	< 500 ms	32 ms See section 5.13	$C_{LOAD} = 1000 \mu\text{F}$
Audible noise	Quiet under all conditions	No audible noise	Cores glued. Transformer varnished.

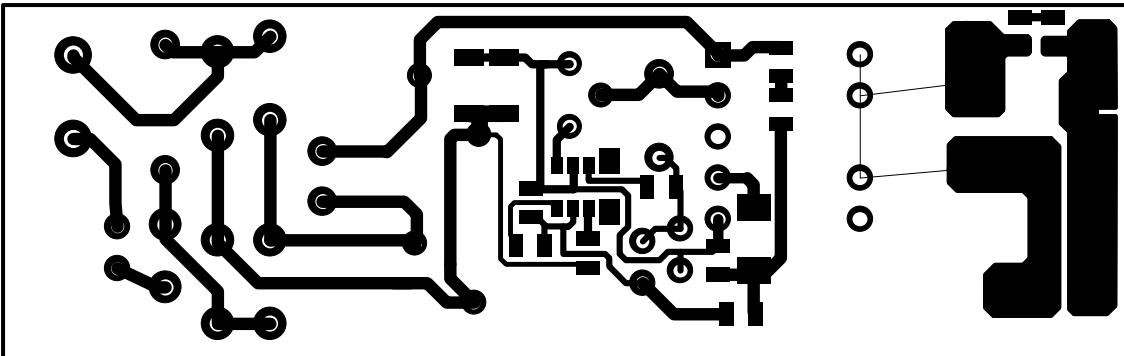
Table 22: Results Achieved With the Example Design

5.5 Example Design – PCB Layout

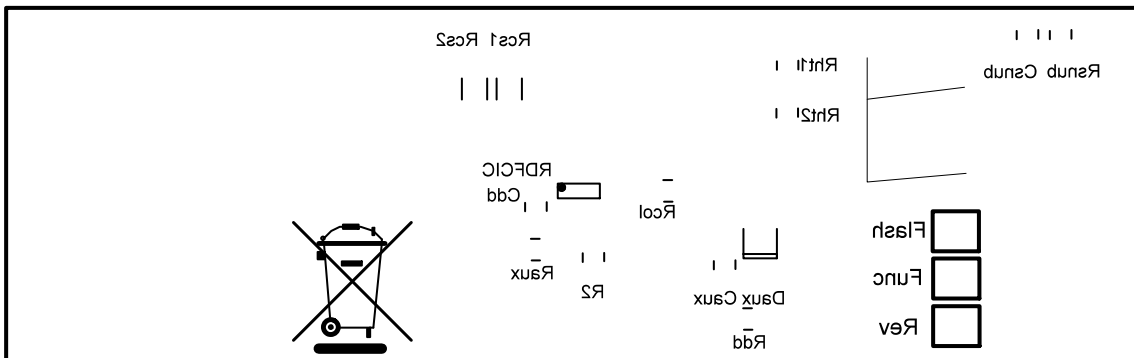
5.5.1 Top Silk



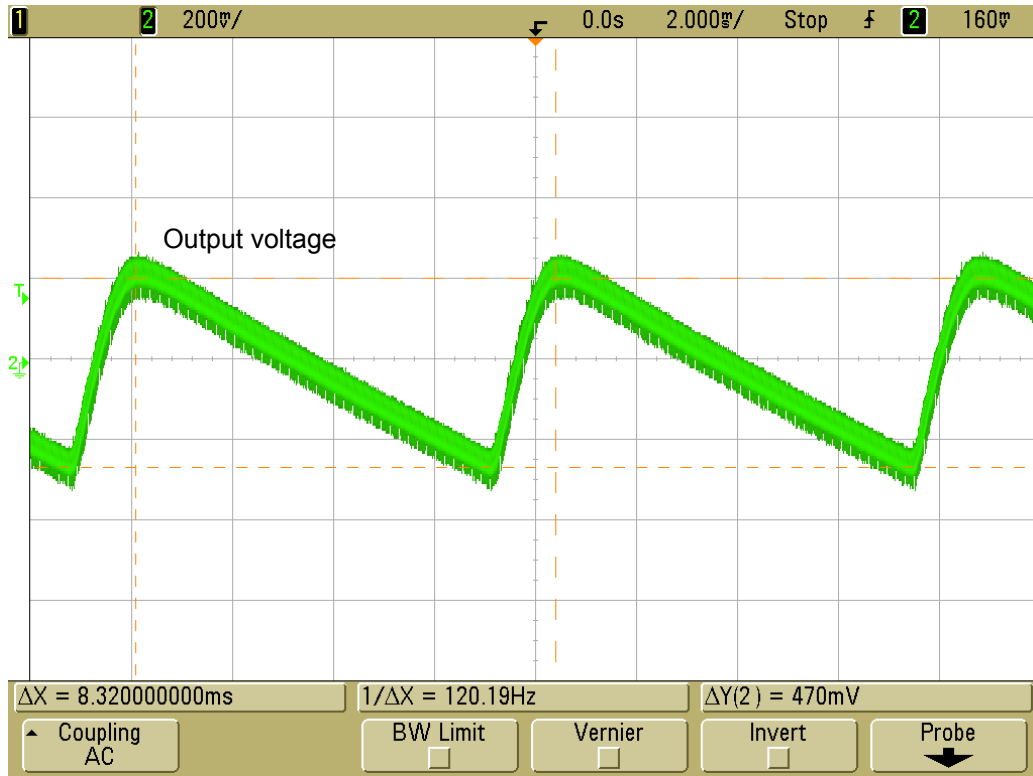
5.5.2 Bottom Copper



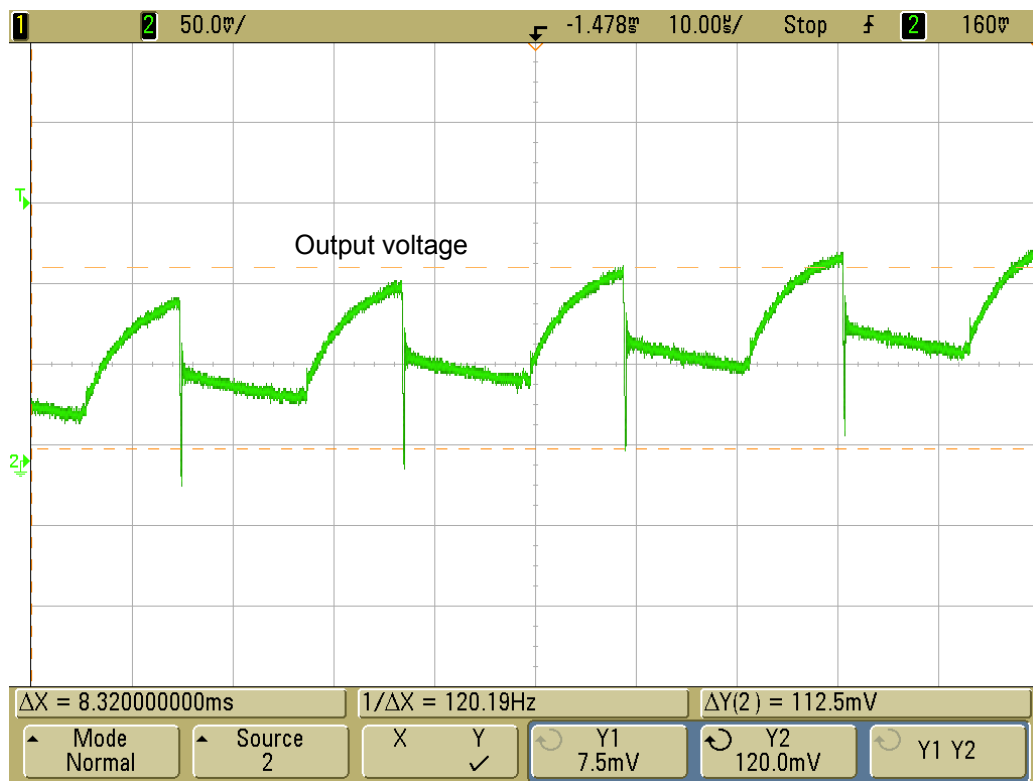
5.5.3 Bottom Silk



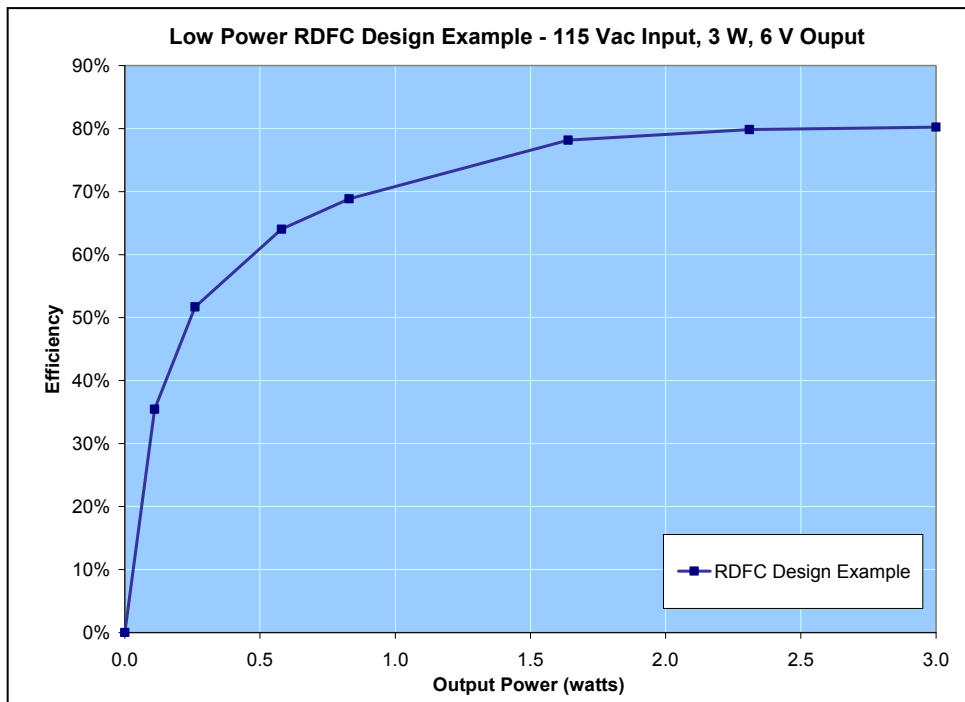
5.6 Line-Frequency Ripple



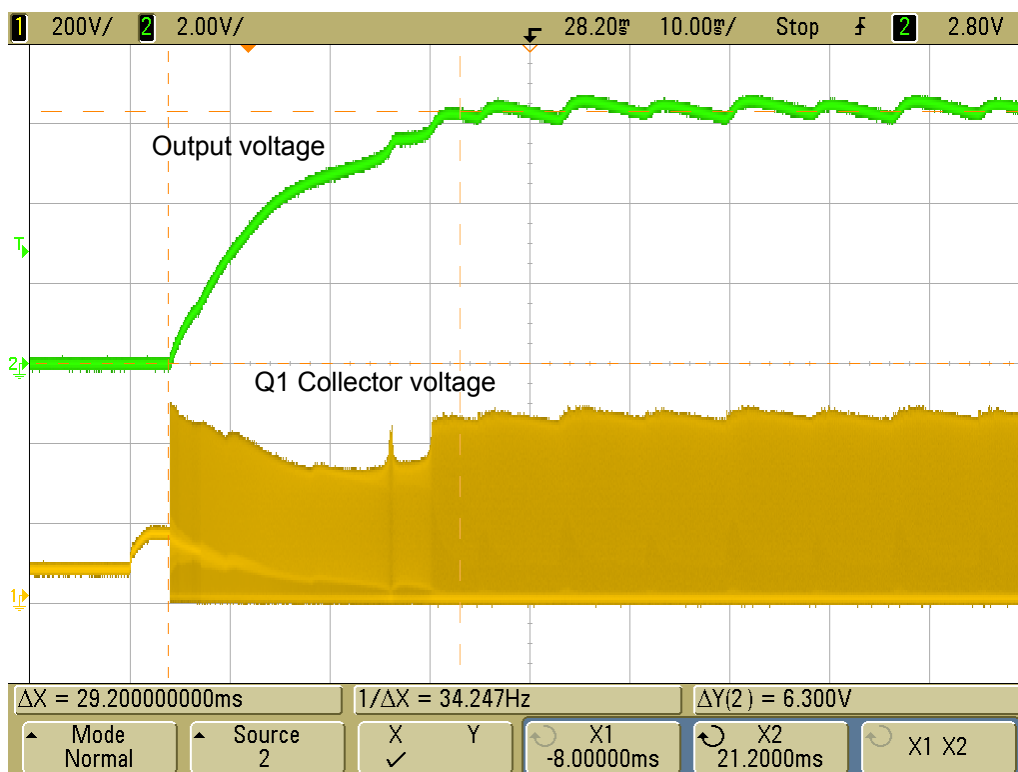
5.7 Switching-Frequency Ripple



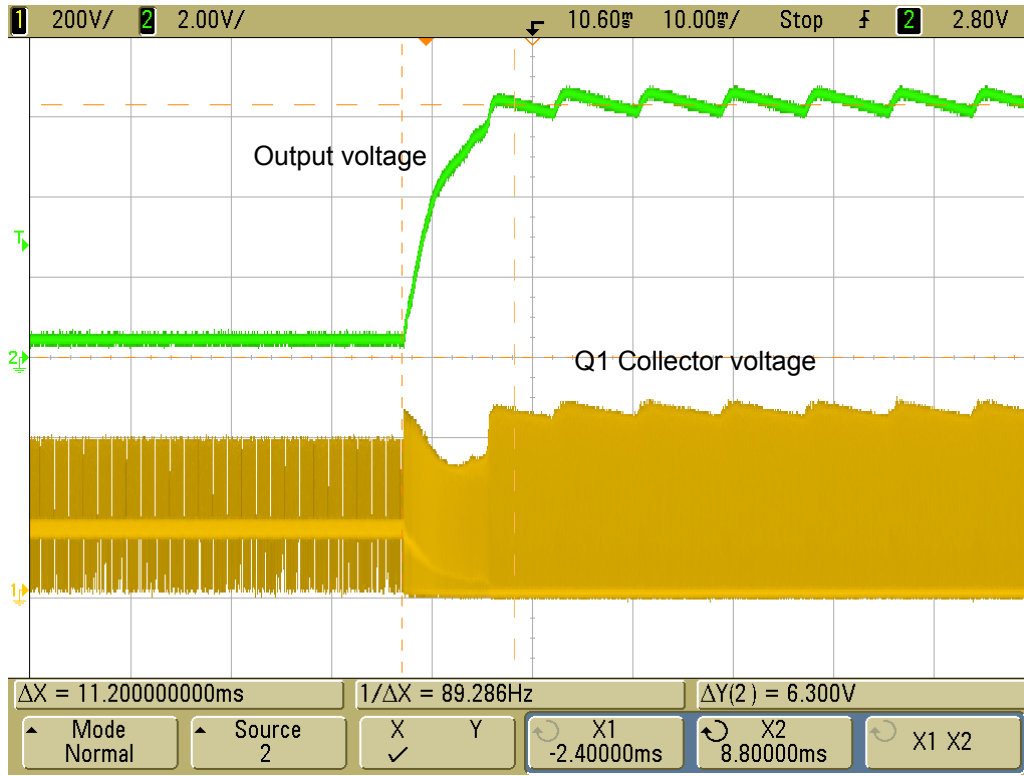
5.8 Efficiency



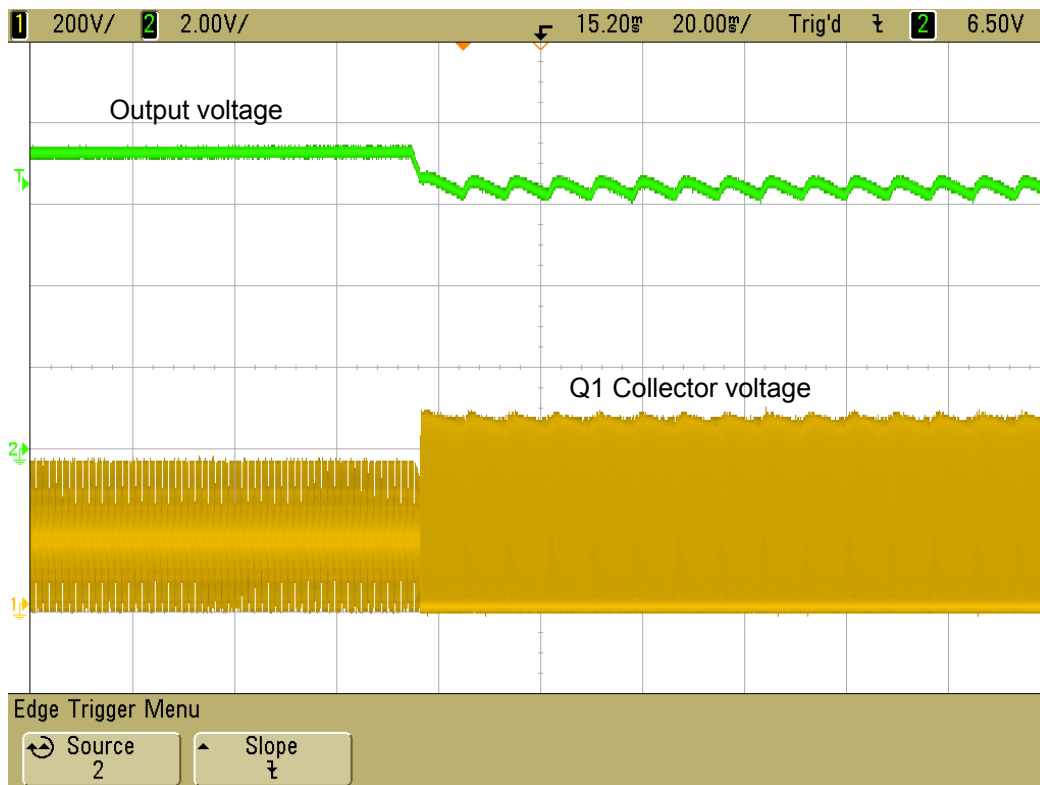
5.9 Load Pull-Up



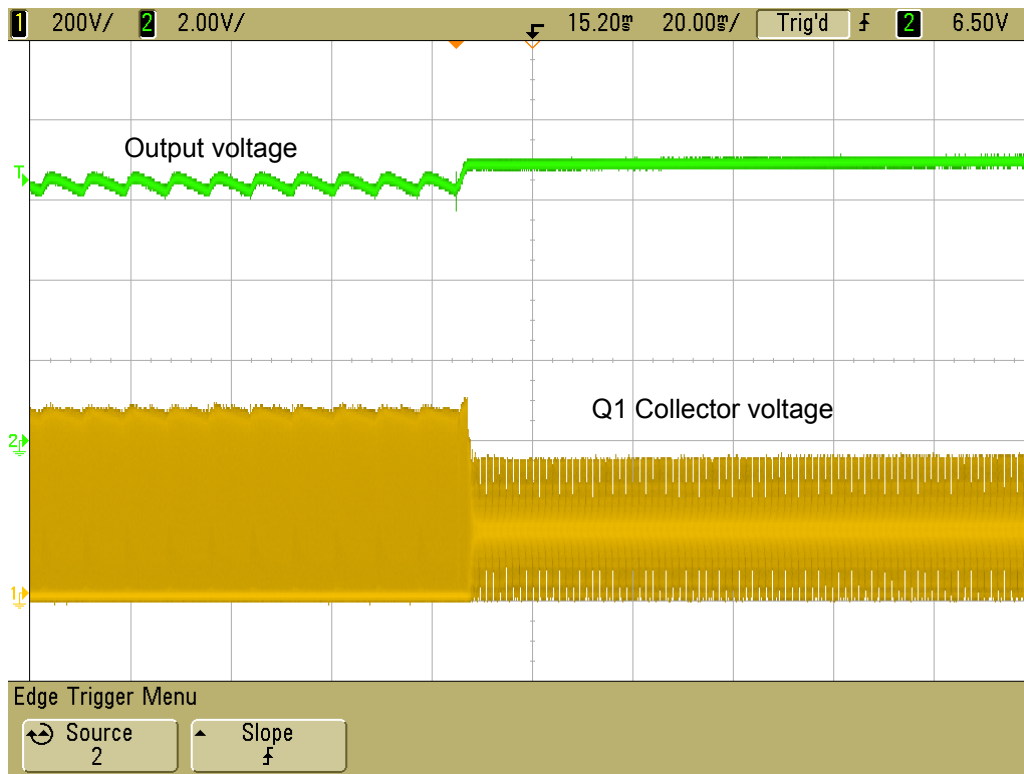
5.10 Recovery from Short Circuit



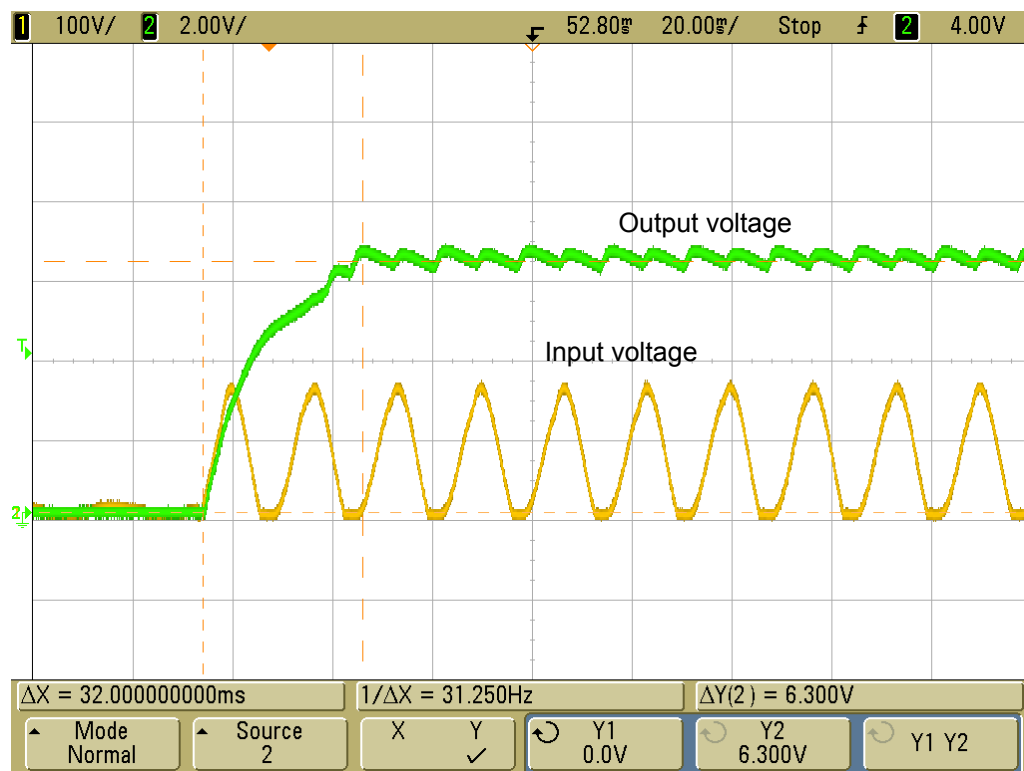
5.11 Load Transient (I_{OUT} Step From 10 mA to I_{NOM}) With Max Load Capacitance



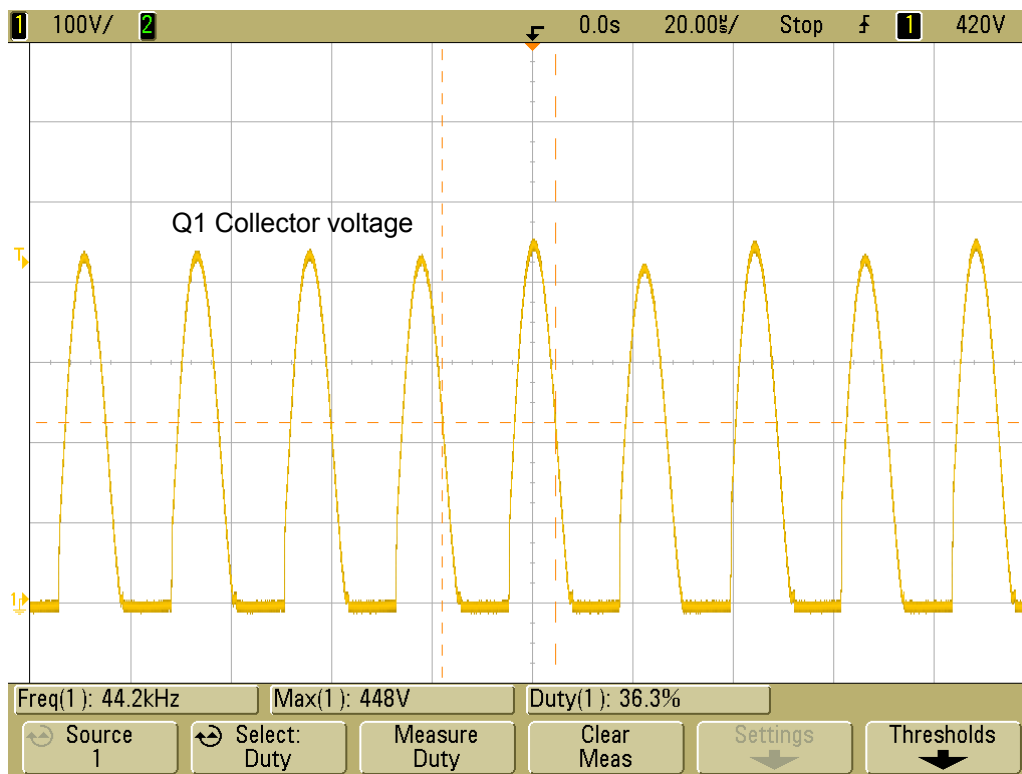
5.12 Load Transient (I_{OUT} Step From I_{NOM} to 10 mA) With Max Load Capacitance



5.13 Turn-on Delay With Max Load Capacitance

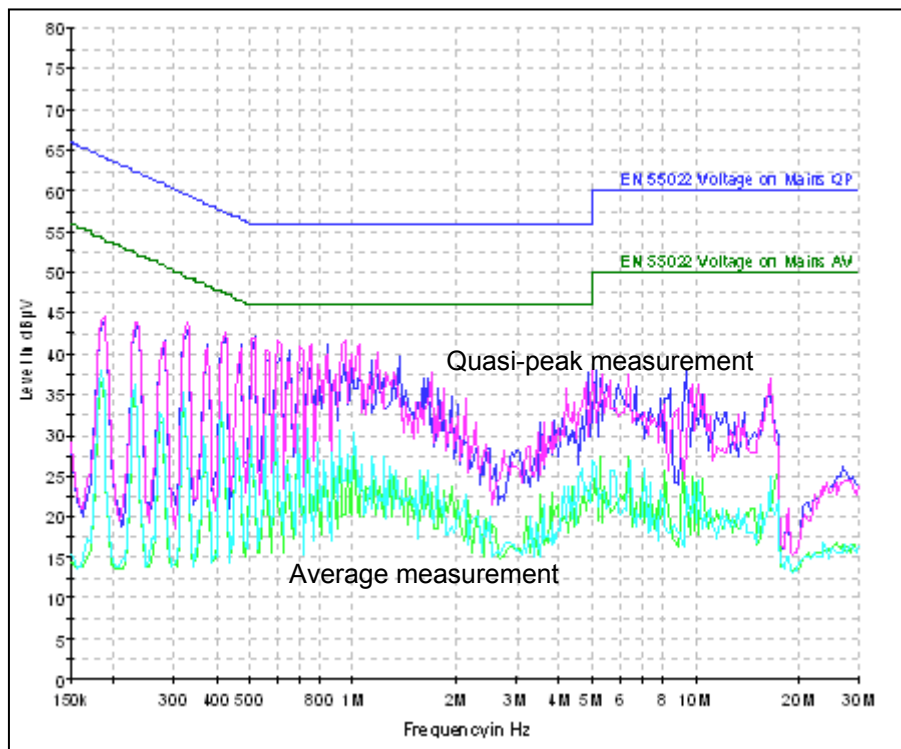


5.14 Operating Frequency (Plot of Q1 Collector Voltage) Measured in Normal Mode



5.15 Conducted Emissions (EN55022 Class B Limits) Pre-Compliance Test

Output 6.3 V, 0.5 A (rated load); 1 nF and 10 Ω snubber across Dout; output grounded; line, neutral.



APPENDIX A DESIGN WORKSHEET

The following worksheets can be used when designing a low power RDFC design with this guide. Please read the following safety advice before undertaking your design.

A.1 Safety

Offline power supplies, particularly in a development situation, can present hazards including, but not limited to, electric shock, high temperatures, fire & smoke. They should be operated and used only by competent, trained personnel. In particular:

- The unit to be tested should be checked for design and build errors before applying mains power;
- The unit under test should be powered via a suitable isolating transformer and a variac;
- Hazardous voltages are present in both normal and abnormal operating conditions;
- Insulation between high voltage and low voltage parts may not provide safety isolation;
- All connections should be regarded as LIVE and HAZARDOUS.

A.2 Specify Your Design Parameters

Use Table 23 to record your basic design parameters.

Design Parameter	Symbol	Typical Range Achievable with Low Power RDFC	Design Target	Comments
Input voltage	V_{IN}	115 Vac (98 to 132 Vac) 230 Vac (196 to 265 Vac)		Application designs are specified for $\pm 15\%$ of the nominal input voltage
Rated output power	P_{NOM}	Up to 6 W		Low power RDFC chip is rated for applications in this power range
Nominal output voltage	V_{NOM}	5 V to 24 V		
Nominal output current	I_{NOM}	0.05 A to 1.2 A		$I_{NOM} = P_{NOM} / V_{NOM}$ Must not exceed upper end of the range achievable with low power RDFC

Table 23: Record Your Basic Design Parameters

A.3 Select Components Using the Design Guide

Use Table 24 to record the components recommended by the guide for your target design parameters

Component		Guide Type/Value/Rating	Refer to Section	Actual Type/Value/Rating
Low power RDFC controller IC		C2471LX2 (SOT23-6)	-	
Dbridge			Section 3.1 on page 5	
$C_{IN} = C_{in1} + C_{in2}$			Section 3.2 on page 5	
Lfilt		1mH	Table 19, page 14	
Transformer core			Section 3.3.1 on page 6	
Secondary turns N_S			Section 3.3.2 on page 6	
Primary turns N_P			Section 3.3.3 on page 7	
Auxiliary turns N_{AUX}			Section 3.3.4 on page 7	
Secondary conductor			Section 3.3.5 on page 8	
Primary conductor			Section 3.3.6 on page 8	
Auxiliary conductor		0.15 mm	Table 12 on page 9	
Primary inductance			Section 3.3.7 on page 8	
Leakage inductance		400 μ H (115 Vac) 1 mH (230 Vac)	Section 3.3.7 on page 8	
Output capacitor Cout	I_{RMS}		Section 3.4 on page 10	
	ESR			
Primary switch Q1			Section 3.5 on page 10	
Resonant capacitor C_{COL}			Section 3.6 on page 11	
Programming capacitor C_p				
Output diode Dout	$I_{F(AV)}$		Section 3.7 on page 12	
	V_{RRM}			
Dcol1 and Dcol2		1N4148	Section 3.8 on page 12	
Rcol		100 Ω	Section 3.8 on page 12	
Rcs			Section 3.9 on page 13	
R2		470 Ω		
Raux			Section 3.10 on page 13	
Rdd		330 Ω	Section 3.10 on page 13	
Fuse		-	Table 19 on page 14	
Rfuse		22 Ω	Table 19 on page 14	
Rht1, Rht2		2.7 M Ω (115 Vac) 4.7 M Ω (230 Vac)	Table 19 on page 14	
Csub	Optimise for EMC performance	1 nF to 2.2 nF	Table 19 on page 14	
Rsub		10 Ω to 100 Ω	Table 19 on page 14	
Rout - optional		1 k Ω /V output	Table 19 on page 14	
Cdd		1 μ F	Table 19 on page 14	
Daux		1N4148	Table 19 on page 14	
Caux		470 nF	Table 19 on page 14	

Table 24: Record the Components Recommended by the Design Guide and Those Actually Used

A.4 Measure the Performance of Your Design

Use Table 25 to record the measured performance of your design. Unless otherwise stated, use the following operating conditions:

- $V_{IN} = 115 \text{ Vac}$ or 230 Vac , depending on your design target
- Power in to the load $P_{OUT} = P_{NOM}$ (rated power)
- Resistive load (capacitance $C_{LOAD} = 0$)

Parameter	Expected Performance	Achieved Performance	Conditions
Output voltage (V_{NOM})	As selected for your design target		
Average efficiency (η)	> 75%		Average of efficiency at 4 load points: 25%, 50%, 75%, 100% of rated power P_{NOM}
Load regulation	<20 % of V_{NOM}		Load current range from 10 mA to I_{NOM}
No load power (P_{STBY})	< 300 mW		No load
Output line ripple	10 % of V_{IN} for $V_{IN} = 115 \text{ Vac}$ 5 % of V_{IN} for $V_{IN} = 230 \text{ Vac}$		At twice line frequency
Output switching ripple	2.5 % of V_{NOM} (pk-pk)		At switching frequency
Load pull up capability	Should pull up constant resistance load		$C_{LOAD} = 1000 \mu\text{F}$
Operating frequency	Typically 50 kHz		
Overcurrent protection	Transition to Foldback mode occurs between $1.3 \times I_{NOM}$ and $1.5 \times I_{NOM}$		
Conducted emissions	EN55022 class B compliance with 6 dB margin		
Short circuit P_{IN}	< 2 W		
Load transient response	Stable operation. Output should remain within max-min regulation.		$C_{LOAD} = 1000 \mu\text{F}$
Turn-on delay	< 500 ms		$C_{LOAD} = 1000 \mu\text{F}$
Audible noise	Quiet under all conditions		Glued cores. May require varnishing.

Table 25: Record the Measured Performance of Your Design

DESIGN GUIDE STATUS

Application design information and specifications provided in this Design Guide (e.g., circuit schematics, board layouts and custom wound component drawings) have not been fully developed for production and have not been subjected to safety or EMC approvals testing. Hence, design information contained herein should not be used for production without further development, verification, validation, approvals and certification appropriate for the intended application.

This Design Guide contains information relating to use of an IC product whose specification is subject to change without notice. Therefore, please always refer to the most current version of this document and the relevant IC product datasheet, available at www.camsemi.com.

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