

INTRODUCTION

Certain primary switch BJT parameters are particularly important for correct operation and long-term reliability of RDFC designs. :

- Current gain (h_{FE})
- Breakdown voltage (BV_{CER})
- Turn-on speed
- Collector capacitance (Cob)
- Reverse bias safe operating area

This application note describes methods for testing and characterising a BJT in respect of these parameters. Refer to application note AN-2337 “BJT Primary Switch Ratings In RDFC Applications” for more information about these parameters (available from www.camsemi.com).

KEY PARAMETERS

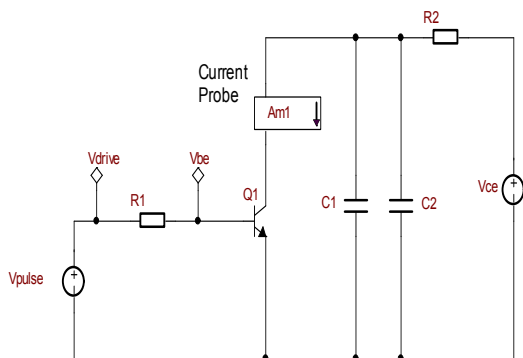
Parameter	Relevance to RDFC-based converters	Comment
h_{FE}	Need to have sufficient base drive available to ensure quasi-saturation otherwise power conversion is ineffective and BJT may overheat	On-state collector voltage is regulated by the RDFC controller (by modulating base current) to achieve an appropriate degree of quasi-saturation. However, this voltage (typically about 2 V for low-line and 5 V for high-line applications) is rarely the same as those used for h_{FE} characterisation in datasheets. Likewise, effects of collector current and temperature have to be taken into account when assessing minimum h_{FE}
BV_{CER}	Relevant voltage rating for RDFC during the resonant off-period	Parameter rarely listed in datasheets but can be shown to be close to BV_{CBO} in RDFC applications.
RBSOA	At turn-off, energy in the transformer leakage inductance is potentially destructive for BJT	Critical issue is the “trajectory” of collector voltage and current during turn off transient. Combination of high voltage and current are destructive. In RDFC, as collector voltage rises, current falls. Capacitance at collector node, and slow transistor turn off limits voltage excursion. RBSOA if specified does not normally cover zero base-emitter voltage condition during turn off. So difficult to relate stated RBSOA to allowable conditions in RDFC converters. A conservative limit has to be applied unless tests show otherwise.
Turn-on speed	To achieve accurate PBD voltage referencing, BJT must reach saturation within short ACTICLAMP period	At BJT turn on in Standby B mode, collector voltage is falling from HT (rectified mains voltage), so takes some time. Though the transformer primary current is low and inductive, there is appreciable capacitance to be discharged. In normal/overload modes, the required fall is smaller but there are greater (and more resistive) load conditions on the collector. This relates to the time-dependent quasi-saturation behaviour.
Cob	Total collector node capacitance is important during turn on, turn off and resonance	Parameter strongly dependent on V_{CE} , but how it changes is rarely specified on datasheets. Also, division between C_{bc} and C_{ce} is significant for consideration of turn on behaviour.

TEST METHODS

This section describes test methods for the parameters identified above and examples of test setups / circuits. It should be noted that most transistor parameters have a significant sensitivity to temperature. The dissipation in the transistor during the tests can raise the die (junction) temperature so it is important that the tests are performed in a way that minimises power dissipation to avoid uncertainty in die temperature. A good way to do this is to operate in pulse mode, with narrow pulses at a low repetition rate (e.g. 10µs pulse width, 10 Hz).

h_{FE}

Commercial curve-tracers are available to plot h_{FE} curves. It is important that these are operated in pulse-mode to avoid self-heating of the die. An alternative method is to use a pulse generator and oscilloscope with the simple test circuit below.



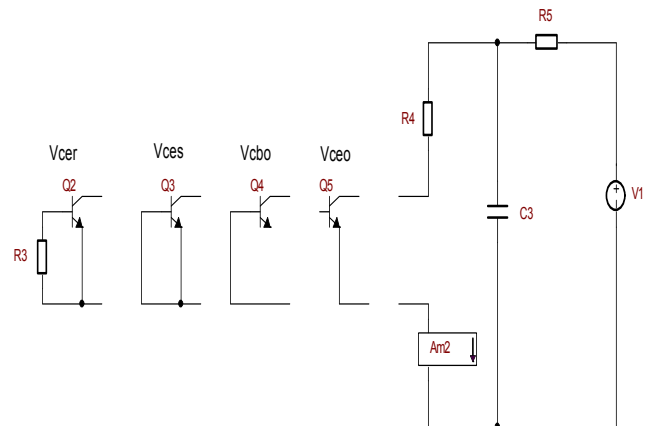
Test Circuit Description: The transistor is operated at a fixed collector bias voltage from a DC power supply V_{ce} . Reservoir capacitors $C1$ and $C2$ ensure constant collector voltage during the test pulse, and resistor $R2$ provides protection in case of failure. A base current pulse is applied from a pulse generator through a current limiting resistor $R1$. The oscilloscope is used to record drive voltage (V_{drive}), base-emitter voltage (V_{be}) and collector current via a current probe ($Am1$). Instead of a current probe, it may be possible to use a low-value resistor in either the collector circuit (sensed differentially) or the emitter circuit. In the latter case, the contribution of base current has to be subtracted for calculation of gain. Resolution of the measurements can be improved by using an averaging mode in the oscilloscope. It is important to avoid errors due to turn on effects and this is best done by limiting the measurement window to the stable portion of the pulse immediately before turn off. It may be necessary to buffer the output of the pulse generator to achieve sufficient base drive current; an emitter follower should be sufficient for this.

Test Method: Gain is affected by collector current and voltage. It is most critical at high collector currents and the test should be performed at typical application collector voltage (PBD voltage). Measurement of this single condition should be sufficient so a fixed base current pulse can be applied. The acceptance condition is a collector current pulse above a threshold value.

Temperature and collector voltage have strong influences on transistor gain, so to achieve consistent / repeatable results it is important to keep temperature and collector voltages constant at pre-determined values.

BV_{CER}

The diagram below shows a simple test circuit for checking BV_{CER} . It can also be used to test BV_{CES} , BV_{CBO} and BV_{CEO} .



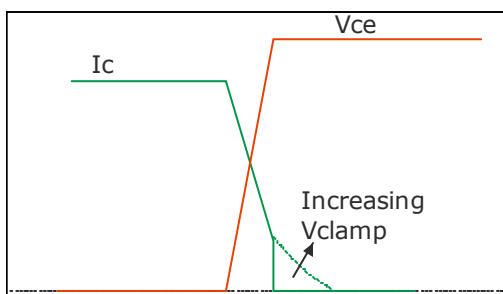
Test Circuit Description: All of these parameters can be measured with a similar test circuit. High voltage power supply, $V1$, is used to apply a voltage between the collector and other terminal(s) of the transistor. Current flow through the transistor is measured using a micro-ammeter ($Am2$). $R4$ (e.g. 100 kΩ) is included to limit current flow when the transistor breaks down, and the low-pass filter $R5/C3$ limits the rate of collector voltage rise – the filter should have a time constant greater than 100 ms to avoid fast rise of collector voltage in this test.

Test Method: The transistor under test is connected in one of the various configurations shown. For testing BV_{CER} , use a preset base-emitter resistor and apply the pre-determined minimum breakdown collector voltage. Check for collector current less than a threshold value (e.g. 50 µA). Note that semiconductor theory may predict an increase of BV_{CER} with temperature, but experimental observation has shown a fall with temperature for some parts.

Note that measurement of V_{CE0} is very sensitive to rate of collector voltage rise, due in some part to the collector base capacitance. Therefore, the rise rate should be clearly defined in the test specification.

RBSOA

Reverse Bias Safe Operating Area (RBSOA) data is often not provided by transistor manufacturers and, if provided, is under conditions very different to those produced by CamSemi’s RDFC controllers. It is necessary to measure turn off characteristics under relevant conditions. At turn off, the voltage and current waveforms are typically of the form shown below.



Collector current falls and collector voltage rises until the clamp comes into operation. The presence of significant collector current after the clamp has come into operation indicates a risk of RBSOA-type failure.

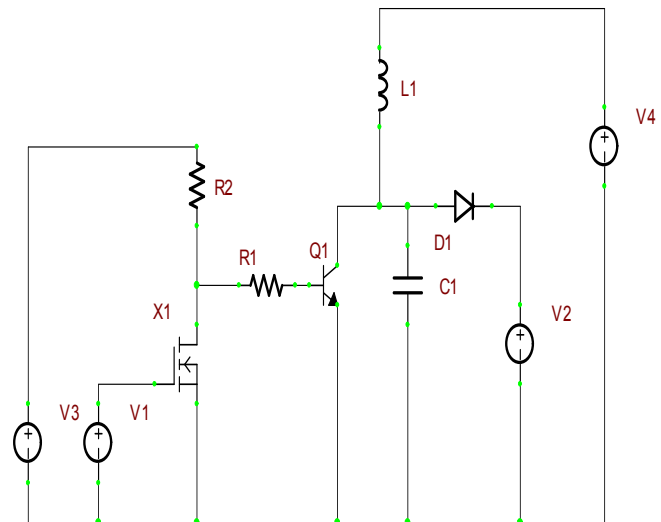
Test Method: The test conditions (I_b , I_c , dV_{ce}/dt) should be derived from worst-case conditions expected in applications. Highest stress in applications normally occurs at high die temperature so it is necessary to adapt the acceptance threshold to compensate for the test being done at room temperature. This can be done by using a higher clamp voltage.

In order to obtain relevant results, it is necessary to test under preset conditions for:

- temperature
- initial collector current (set by the combination of on-period, L1 value and V4 voltage)
- turn-off resistance ($X1 R_{ds} + R1$)
- rate of collector voltage rise (set by initial collector current and C1 value)
- clamp voltage (V2)

The acceptance criterion can be to test that collector current is lower than a threshold value at a fixed delay after turn off. Current in the collector of Q1 is monitored using a current probe and oscilloscope.

The diagram below shows a test-circuit that can be used to evaluate RBSOA.



Test Circuit Description: Q1 is the transistor under test. V2, V3 and V4 are DC power supplies; V1 is a pulse generator to turn the transistor on and off. MOSFET X1 mimics the shunt off transistor in the controller; the drain resistance, together with R1, corresponds to the maximum resistance of the shunt off transistor. V1 provides a narrow negative going pulse to turn off X1 so base current is applied to Q1 from V3 via R2 and R1. Q1 turns on and current builds up through inductance L1. At the end of the pulse from V1, X1 turns on, removing base current and connecting R1 as a discharge path from the base of Q1 to the emitter. After the storage time of Q1, the collector voltage rises at a rate limited by the capacitance C1 and the current through L1. To achieve fast dV/dt it is important that L1 has a low capacitance. The collector voltage is limited by the clamping action of D1 and V2.

Turn-on Speed

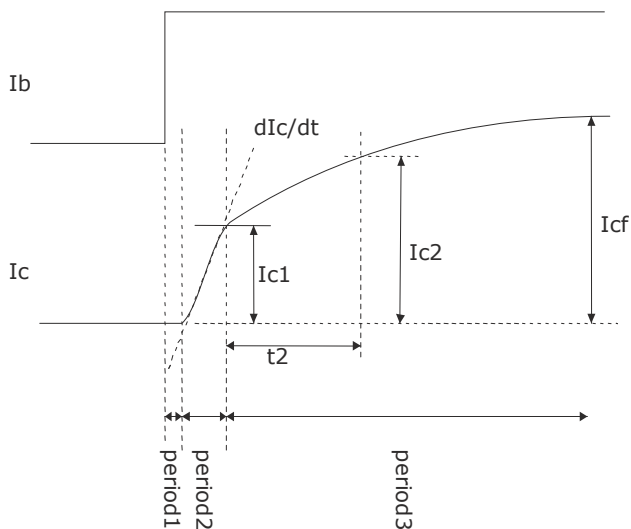
Two important turn-on characteristics that should be evaluated are:

- Initial (fast) rise of collector current
- Quasi-saturation resistance and time constant

They can be measured with the same test circuit as for h_{FE} , the difference being that collector current data is taken from the initial (turn on) part of the pulse rather than the trailing part or steady part of the pulse which is used for h_{FE} measurement. A typical waveform is illustrated below and exhibits three phases.

- 1: Delay T_d , while the base region charges
- 2: Fast rise of collector current up to a limit I_{c1}

3: Continuing rise of I_c , but at slower time constant, to I_{cf} (not shown). A sampling point on the curve (t_2/I_{c2}) can be used to check turn on performance.



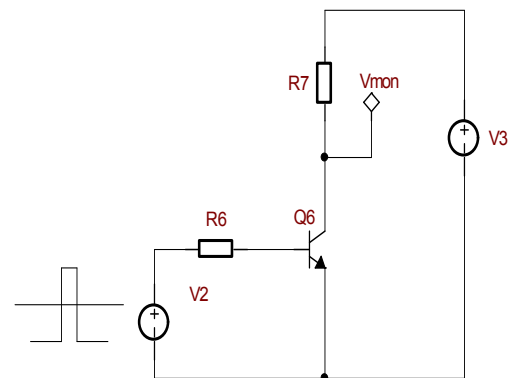
Test Method: Instead of checking all of the various turn on speed parameters, a simplified test could simply check for collector current above a threshold value at a time sampling point shortly after turn on. The delay time for the sampling point can be chosen so that it is sensitive to changes of quasi-saturation resistance and time constant. It will be necessary to adapt the production test threshold to account for temperature, since worst-case conditions occur at high temperature in applications. This test can be combined with the h_{FE} test.

Cob

Two capacitances are of interest:

1. Total collector capacitance (relevant to resonance frequency, rise of collector voltage from leakage inductance energy & turn on of BJT from non-zero collector voltage)
2. Collector-base capacitance (limits the turn on speed because of Miller effect)

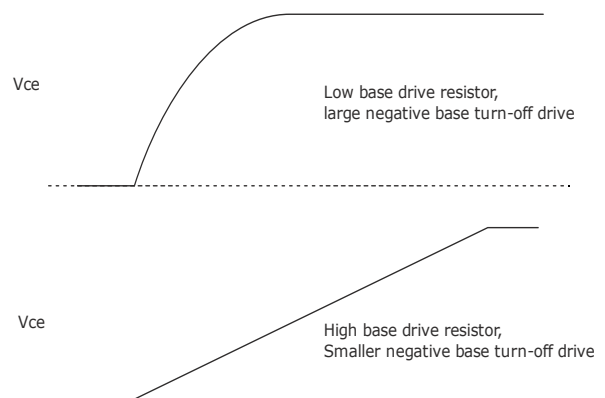
In some transistors, there may be very little difference between the two values because virtually all capacitance is between base and collector. It is useful to measure these at high collector voltage, rather than the low voltage commonly used for datasheet specifications. These can be measured using the simple resistive turn off circuit below.



Test Method:

a) For C_{ob} measurement, the base drive resistor R_6 is chosen so that the transistor is turned off with a large negative base drive. The rising collector waveform is simply the exponential form from the time constant = $R_7 \cdot C_{ob}$. The capacitance can be estimated either by measuring the time constant or from rate of collector voltage rise at a point on the curve, and resistor current calculated from collector voltage, supply voltage and value of R_7 .

b) For C_{bc} (base-collector capacitance) measurement, a large R_6 is chosen, so the rate of collector voltage rise is limited by the Miller effect in the transistor. In this case, the base collector capacitance is calculated from the rate of collector voltage rise, and calculated current in resistor R_6 .



Note that both capacitances change with collector voltage and should be evaluated at a relevant voltage (e.g. HT voltage of a typical application).

Collector capacitance is not expected to change greatly with device temperature, which simplifies setting the acceptance thresholds. Using the test setup described above, the collector voltage is sampled at a fixed delay after the end of the base pulse. The measured voltage is compared against maximum and minimum values.

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