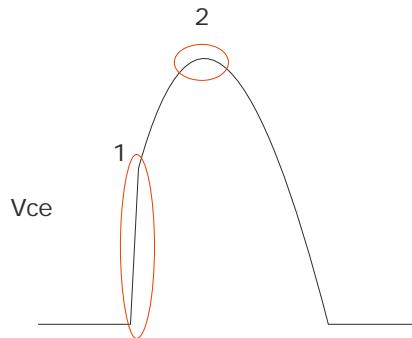


INTRODUCTION

In RDFC applications, like all switch mode power supplies, it is important to characterise and tune designs to ensure adequate safe operating margin of the primary switch. This application note explains how to measure collector voltage under the most stressful conditions of circuit operation. Relevant transistor ratings are discussed in application note AN-2337 (available from www.camsemi.com), which we recommend should be studied before reading this application note and before selecting a BJT for RDFC applications.

KEY ASPECTS OF THE COLLECTOR VOLTAGE WAVEFORM

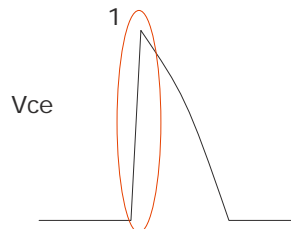
Two key aspects of the collector voltage waveform must be considered in RDFC applications:



1. Fast rise of collector voltage at turn off (“Vkick”) when collector current may still be flowing
2. Maximum collector voltage during resonance (“Vresmax”), when collector current is very low

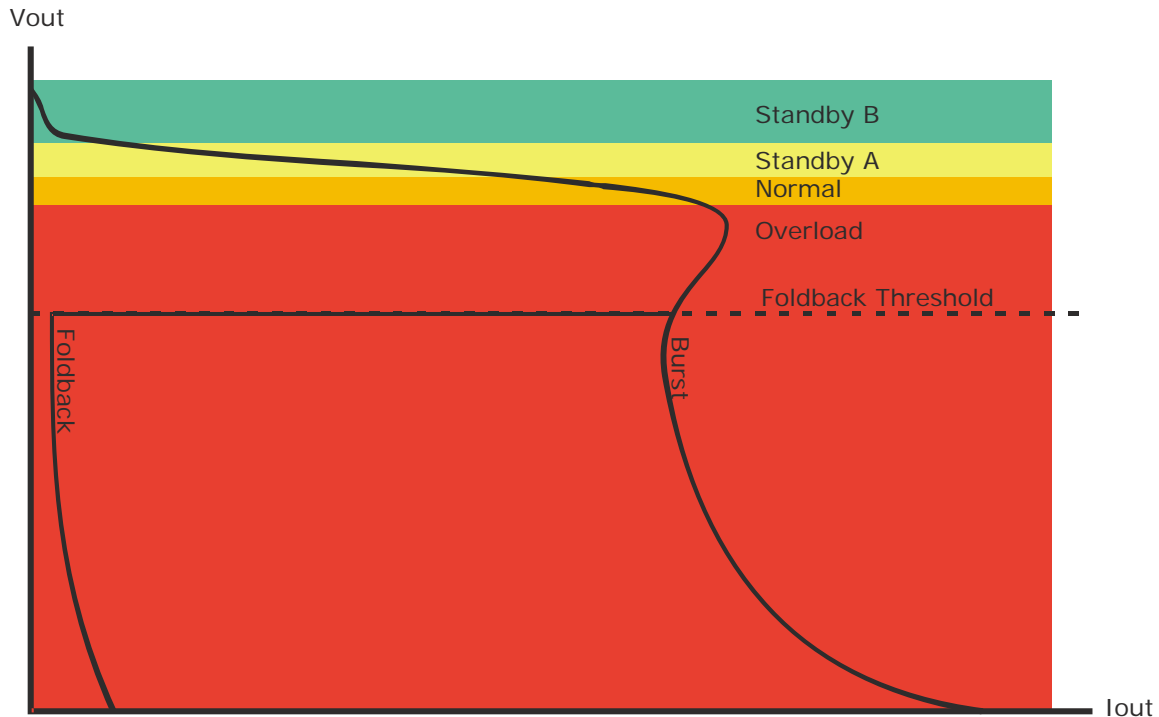
Conditions inside the transistor are very different in these two parts of the waveform. The BJT behaves differently and different transistor ratings are relevant. RBSOA is a particularly important consideration as collector voltage starts to rise (1) and V_{cer} is a key rating at the peak (2). Refer to AN-2337 for information about RBSOA and V_{cer} .

Note that, when the power supply is heavily overloaded, waveform may change to resemble:



The operating conditions of the transistor vary considerably across the load range of the power supply. This document explains how to measure collector voltage under the most stressful conditions of circuit operation.

RDFC OPERATING MODES



The C2470 series RDFC controllers have operating modes that are selected according to where the converter is operating on the V-I characteristic, as described in the IC datasheet. Note that the controller “Standby” operating mode is in fact two modes:

Standby B (No-load to Low load range): On-time is held at a constant minimum, off-time reduces as load increases. Once the off-time reduces to the resonance time, the converter changes to Standby A mode

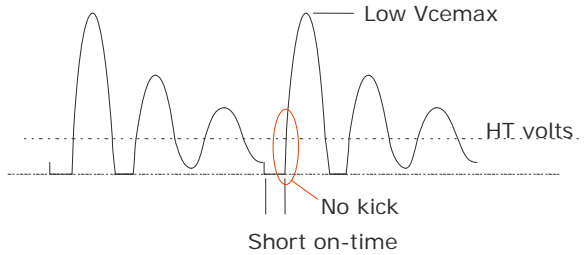
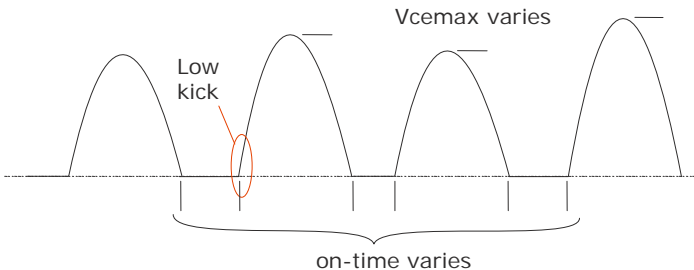
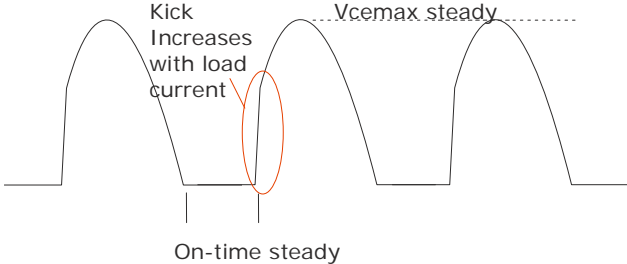
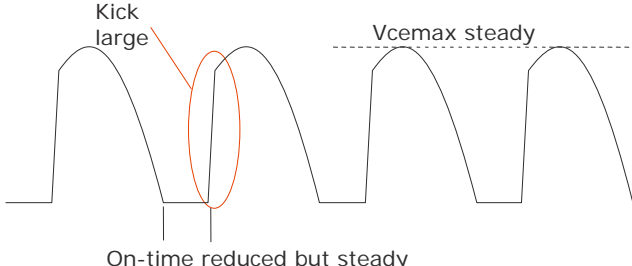
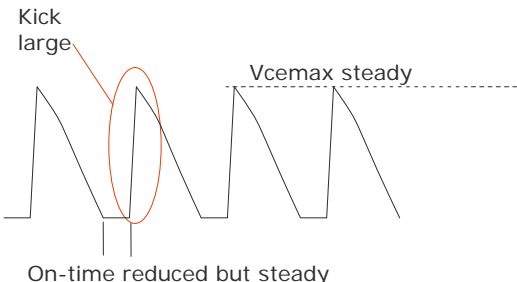
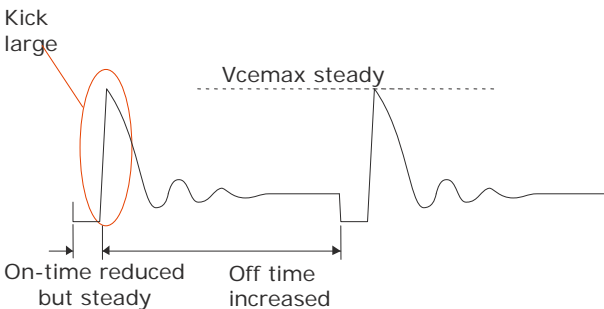
Standby A (Low load to Medium load range). Off-time matches the resonance time and on-time increases with increasing load.

The switch collector voltage waveform varies according to the operating mode as shown in the following diagrams.

Note: “Kick” = fast rise of collector voltage at turn off due to energy (current) in the transformer leakage inductance.

RDFC-based converters usually have substantial ripple voltage on the HT supply. This causes varying difference between transformed input voltage and the output voltage, which in turn triggers variation of the mode of the controller (particularly on-time). So we will normally see the controller moving between modes throughout a ripple cycle.

Foldback/burst operation is triggered when the output voltage is below the foldback threshold voltage so that the on-time is reduced below the foldback threshold time (see datasheet). Operating waveforms in Burst mode operation are the same as Normal or Overload (depending on the output voltage). Foldback mode is different only because the off-time is increased by the controller to reduce the output power; the on-time, turn off and (initial) resonance waveform are the same as Normal/Overload (according to output voltage).

<p>Standby B</p>	
<p>Standby A</p>	
<p>Normal</p>	
<p>Overload</p>	
<p>High overload</p>	
<p>Foldback</p>	

EFFECT OF OPERATING CONDITIONS ON COLLECTOR VOLTAGE

Operating conditions are affected both by output voltage and line input voltage. Rate of rise of current during the on-period depends mostly on the difference between the transformed input voltage and the output voltage. When the load is low, current at turn off is also low. It increases as load current increases then is limited by OCPH in overload. In overload there is some increase in current at turn off when the output voltage is reduced, caused by delay in BJT turn off. The current at turn off determines the rate of rise of and the peak value of the "kick" voltage (V_{kick}).

Peak resonance voltage is caused by transfer of energy from the magnetic core to the resonating capacitor. So the peak voltage depends on the peak core magnetisation which, in turn, is determined by

- Input voltage
- On-time
- Transformer parameters
(core type, gap, primary turns)
- Core magnetisation from the previous converter cycle

For a fixed on-time, higher input voltage causes more core magnetisation which gives higher resonance voltage (V_{resmax}). During the on-time the magnetising current increases linearly because of the HT voltage applied across the magnetising inductance, so longer on-time causes more core magnetisation. When the converter is operating resonantly i.e. the transistor turns on immediately the collector voltage has returned back to 0 V, there is reverse core magnetisation at the beginning of the on-time. When the transformer is resonating in the off period, current in the magnetising inductance is the same as the current in the resonating capacitor; positive current in the magnetising inductance causes the capacitor voltage to rise, falling capacitor voltage means the magnetising current is negative. In typical resonant operation, the core magnetisation is **negative** at the **beginning** of the on-time and rises linearly to a **positive** magnetisation at the **end** of the on-time. During the resonant off-period the resonance causes the magnetisation to reverse before the next on-period. **Peak collector voltage in the resonance period depends on the maximum magnetisation at the end of the previous on period.** High magnetisation can be caused by:

- High supply volts
- Longer on-time
- Lower (magnitude) of negative magnetisation at the beginning of the previous on period (i.e. less negative)

In conditions where the on-time is varying, the peak resonant voltage will also vary because of the:

- Increase of magnetisation during the on period
- Variation in negative magnetisation at the beginning of the on period

Highest magnetisation occurs when the on-period is longest and the previous on-period is shortest. A short previous on-period means that the negative magnetisation is low in magnitude at the beginning of the next on-period.

In addition to changing on-time set by the controller, charge storage in the transistor can also cause increased on-time. Long charge storage times can be caused by inappropriate setting of the PBD voltage or high F_{on} current. Note also that storage time tends to increase with increasing transistor temperature.

CRITICAL CONDITIONS FOR TRANSISTOR VOLTAGE STRESS

It is necessary to check both V_{kick} against RBSOA, and V_{resmax} against V_{cer} . The two different types of voltage stress vary with the converter operating conditions. It is necessary to operate the converter under different conditions to find the worst voltage stresses of each type experienced by the transistor.

We also need to take account of the change in the transistor's withstand ability with, for example, temperature. When temperature changes in the application there are some changes in the operating conditions but there are also changes in the ability of the transistor to withstand stress. We are normally interested in the margin between stress applied to the transistor and the ability of the transistor to withstand the stress. When both of these are changing it is often unclear what the worst-case conditions are. Increased transistor temperature typically reduces withstand ability in both RBSOA and V_{cer} modes. It also increases charge storage, so currents at turn off (both in the magnetising inductance and in the leakage inductance) typically rise. This usually means that the worst stress on the transistor happens when the transistor is hot (high currents at turn off and lower ability of the transistor to withstand the stress).

V_{kick} and RBSOA

See AN-2337 for a discussion of RBSOA. In this context transistor stress is a combination of fast rise of voltage and collector current. Worst conditions happen when the current at turn off (end of the on-period) is highest. Typically this happens at:

- High line input voltage
- Low output voltage (e.g. short-circuit load)
- High transistor temperature (slower turn off causes higher peak current)

These conditions can occur either when the output of a power supply is shorted or by starting up a power supply into discharged output/load capacitors or into a short circuit.

High transistor temperature also increases the susceptibility of the transistor to RBSOA failure. However, in a particular application the highest transistor temperature may not occur in short-circuit conditions. Often the highest temperature occurs at the lowest output voltage that does not quite trigger foldback. In this condition the converter operates continuously at high current with very short on-time and this causes maximum transistor heating.

To evaluate stress against RBSOA it is necessary to measure the combination of collector current and collector voltage during the turn off event. Note that it is not possible to do this by monitoring emitter current because there is substantial negative base current under these conditions. Instead it is necessary to monitor the collector current using a current probe. See AN-2337 for more details.

V_{resmax} and V_{cer}

Maximum resonance voltage normally occurs when the on-time is **increasing** on a cycle by cycle basis up to a maximum on-time. When the on-time is increasing, the negative magnetisation from the previous cycle is lower (in magnitude) than for continuous operation at a constant on-period. This behaviour is found in the transition from Standby A to normal mode. When this transition coincides with high HT voltage (near the peak of the ripple voltage), the resonant voltage will be maximum. A convenient method to measure this is to use an oscilloscope to monitor the collector voltage waveform. With trigger mode set to "normal" the trigger threshold is set to a high value so that it only just triggers on the peaks of the resonant voltage. The converter is then operated from maximum mains voltage and a constant current load is adjusted to find the worst-case operating condition for peak collector voltage. Typically this occurs at 20% to 30% of rated load. By adjusting the load current and the trigger threshold voltage the highest resonance voltage can be found.

The effects of long charge storage on peak resonant voltage can also be investigated by heating the transistor and testing with a reduced R_{aux} resistor.

Other conditions that should also be tested for maximum resonance voltage are start-up into pre-charged output capacitor and under surge conditions, where the HT voltage can increase substantially because of the surge energy. Behaviour of the converter during surge varies between designs and load conditions (e.g. by how much the HT voltage rises and how quickly the output voltage rises as a consequence). So it is necessary to test designs under different conditions (e.g. load type and temperature).

REFERENCES

Visit www.camsemi.com to obtain the latest version of these documents.

- [1] RDFC C2472, C2473 Product Datasheet (DS-1423), www.camsemi.com/support/datasheets
- [2] C2471 Datasheet, RDFC Controllers for Offline Applications up to 6 W (DS-1639), www.camsemi.com/support/datasheets
- [3] BJT Primary Switch Ratings (AN-2337), www.camsemi.com/support/appsnotes

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