Offline Power Supply Design with C2470 RDFC Controller

Application Note AN-2280

ABSTRACT

This application note provides offline power supply design guidelines based on the RDFC topology and CamSemi controller IC family C2470. Key design equations and component selection information is included.

Further information on the RDFC topology and CamSemi's advanced controller IC's is available at www.camsemi.com.

INTRODUCTION

The Resonant Discontinuous Forward Converter (RDFC) topology offers superior performance in terms of efficiency, no-load power consumption and size advantages over conventional hard-switched SMPS designs. It is particularly attractive to the audio and other EMI-sensitive applications, such as cordless phone adapters and modem/router power supplies, due to the inherent low EMI nature of the resonant power conversion.

CamSemi's advanced mixed signal control IC family (C2470) has been developed to ensure the RDFC circuitry operates at optimum performance levels with load variations. The C2470 family of controllers achieves this through three main control mechanisms:

- Resonant control - senses the resonance waveform to identify the near-zero turn-on and turn-off voltages and to determine the optimum on-time in the next switching cycle
- Power control - achieved by sensing the switch current and limiting it under overload conditions or reducing on-time at low load conditions to minimise no-load power loss
- Base drive control - dynamically maintains the power transistor on-state voltage at an optimum voltage to control conduction losses and reduce turn-off time and losses

The RDFC controller uses a combination of these control mechanisms to define five main operating modes of the power supply as shown in Figure 1:

- Normal mode - to provide fully resonant switching with a fixed duty cycle for power delivery from around 20% to 100% load
- Standby mode - as the load decreases, the controller enters Standby mode to reduce on-time and increase off-time, to reduce no-load power consumption
- Overload mode - occurs during high output loads, limiting peak switch current and reducing on-time, while maintaining fully resonant operation
- Foldback mode - occurs during excessive output loads, reducing to a minimum on-time while increasing off-time and protecting the power supply in short circuit conditions
- Power burst mode - entered periodically during Foldback mode to allow the power supply to recover from a short-circuit condition, by increasing duty cycle

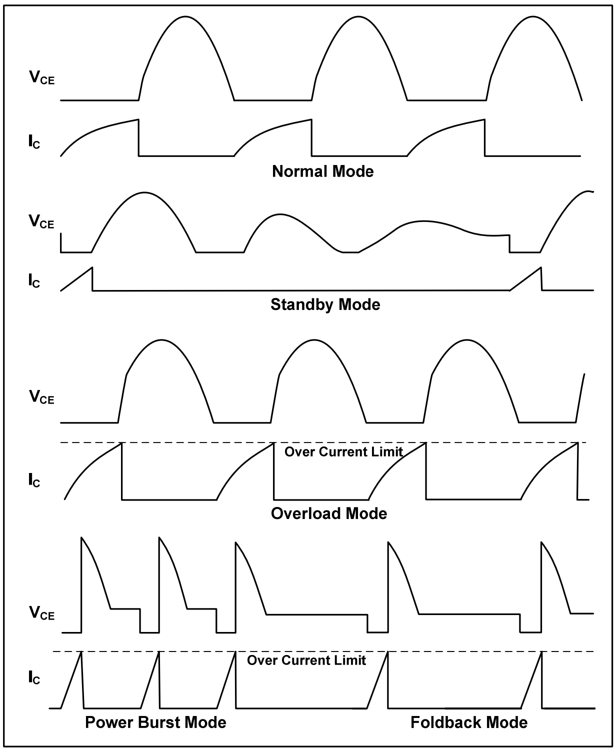

Figure 1: RDFC Operating Modes

TYPICAL APPLICATION CIRCUIT

Figure 2 illustrates a typical RDFC application circuit. The main application sub-circuits are the input stage and pi filter, bootstrap circuit, auxiliary circuit, sense circuits, transformer and output stage.

The input circuit consists of a flame-proof fusible resistor or fuse to provide protection in the event of circuit failure, a thermistor to limit inrush current and an optional MOV to provide surge immunity. Mains voltage is rectified by a full bridge circuit and then smoothed by the bulk capacitors Cin1 and Cin2, which also form a pi filter with Lfilt to reduce differential mode conducted EMI.

Rht1 and Rht2 provide V_{DD} supply at start-up until the auxiliary supply is established. A decoupling capacitor, Cdd, is used to avoid excessive V_{DD} fluctuations during start-up and aid V_{DD} regulation.

The auxiliary voltage is rectified and smoothed by Daux and Caux respectively. Rdd limits V_{DD} current and excessive dissipation in the controller IC shunt regulator . Qaux is turned on only when the base drive is on and allows limiting/programming of the maximum base current with Raux.

Resonant control and base drive control in the RDFC controller are achieved using the COL pin, which senses the transistor (Q1) collector voltage through Ccol. Off-state collector voltage sensing allows accurate detection of near-zero turn-on and turn-off voltages, and allows the optimum on-time to be determined. On-state collector voltage sensing allows the transistor to be maintained in quasi-saturation mode. Cp is used to programme the on-state collector voltage.

Power control is achieved using the CS pin, which senses the transistor (Q1) emitter current. Rcs allows the OCPH threshold to be set. R2 sets the OCPL threshold. The OCPH threshold sets the peak Q1 emitter current so protecting Q1 and the power supply under overload conditions. OCPL sets the standby-normal mode threshold and provides control of the no-load power dissipation.

The RDFC transformer operates in forward mode and no energy is stored within the transformer during switching, so the RDFC topology gives a core size reduction. The transformer consists of three windings: primary, secondary and auxiliary. Additional screen windings may be required to reduce conducted emissions.

The output stage consists of a rectifier diode, a secondary snubber to reduce common mode conducted emissions generated due to diode snap, an output capacitor for output voltage smoothing and an optional dummy load to limit output voltage rise during no-load conditions.

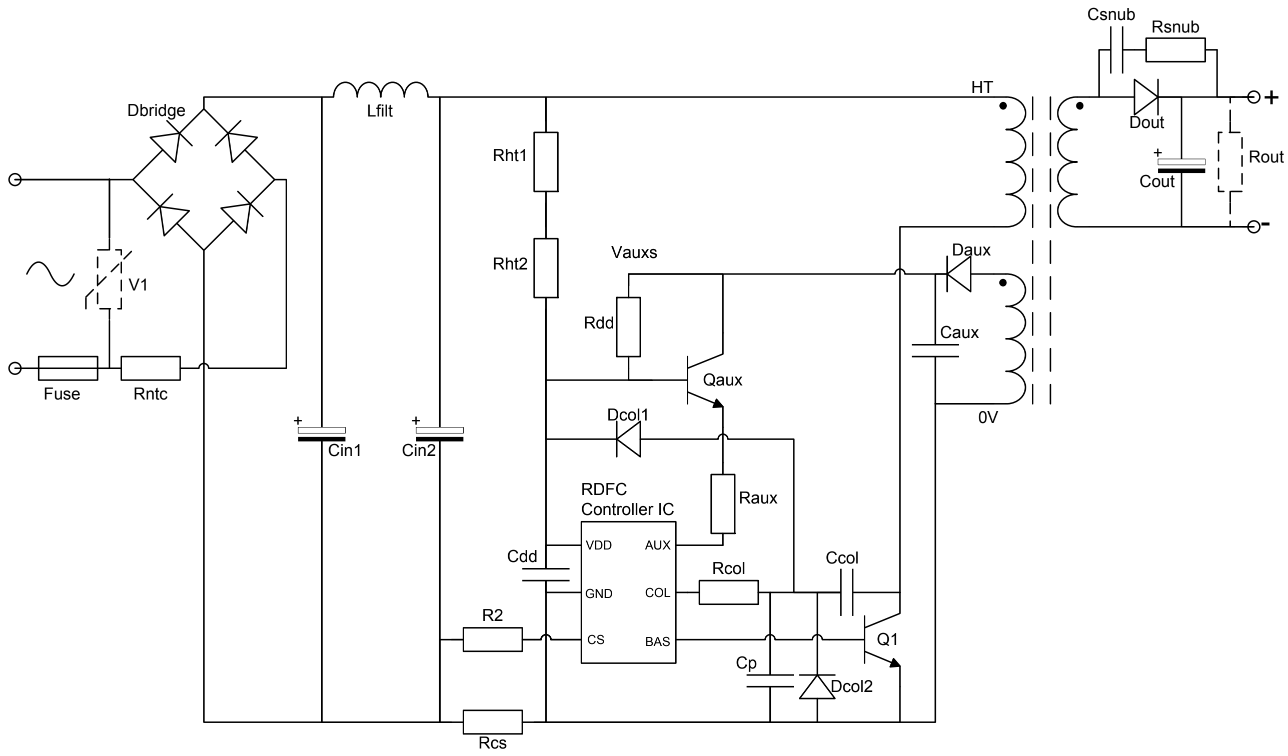

Figure 2: Typical RDFC Application Circuit

COMPONENT SELECTION

The following sections describe the requirements and design equations for determining suitable components for RDFC power supplies. A brief transformer design description is also included.

Line Rectifier (Dbridge)

Depending on the power requirement, cost and PCB area, the input line rectifier can be either four discrete diodes or an integrated bridge rectifier. Maximum forward current (I_{IN}) and minimum repetitive reverse voltage rating (V_{RRM}) are the main parameters to be considered when selecting the line rectifier.

I_{IN} is given by:

$$I_{IN} = \frac{P_{NOM}}{\sqrt{2} \times V_{IN-MIN} \times \eta}$$

P_{NOM} – Nominal output power (W)

$V_{IN\text{-}MIN}$ – Minimum ac input voltage (Vrms)

η – Efficiency (%)

V_{RRM} is given by:

$$V_{RRM-MIN} = 1.5 \times \sqrt{2} \times V_{IN-MAX}$$

$V_{IN\text{-}MAX}$ – Maximum ac input voltage (Vrms)

The factor 1.5 provides allowance for tolerances. Higher margin can be needed to meet specific surge requirements.

Input Capacitance (C_{IN} = Cin1+Cin2)

The value of C_{IN} required depends on the average primary current and peak-to-peak ripple voltage across C_{IN} for a given target output ripple.

C_{IN} is given by:

$$C_{IN} = 0.3 \times \frac{P_{NOM}}{V_{IN-NOM}^2 \times \eta \times f_{LINE} \times Ripple}$$

$V_{IN\text{-}NOM}$ – Nominal AC input voltage (Vrms)

f_{LINE} – Line frequency (Hz)

Ripple – Percentage output ripple

Electrolytic capacitors selected for C_{IN} must have minimum voltage ratings of:

- 200 Vdc for 115 Vac applications
- 400 Vdc for 230 Vac applications

Transformer Design

Transformer design is critical to achieve optimum performance in RDFC power supplies. Key parameters that define a suitable transformer are nominal output power (P_{NOM}), type of load, input voltage, power supply size and target BOM cost.

E cores are preferred due to their features: low cost, compactness, availability in high frequency material, abundance and popularity among SMPS manufacturers. EE13 to EE25 cores in low loss core materials such as PC40 and 3C90 are suitable for RDFC designs from 1 W to 40 W. Ungapped cores are used for low line RDFC designs, while gapped cores are required in high line designs to avoid core saturation and operation below the minimum switching frequency allowed by the RDFC controller. Typical core gaps used in RDFC designs are 50-100 µm.

The minimum number of primary turns ($N_{P\text{-}MIN}$) for a given transformer core and switching frequency is given by:

$$N_{P-MIN} = 1.1 \times \frac{\sqrt{2} \times V_{IN-MAX}}{1.6 \times B_{MAX} \times 7/3 \times f_{SW} \times A_e}$$

B_{MAX} –Maximum flux density (T)

f_{SW} – Switching frequency (Hz)

A_e – Effective core area

Note: This assumes fully resonant operation, core flux swing from -60% to 100% of B_{MAX}, maximum input voltage and +10% allowance for tolerances.

The number of primary turns can be adjusted to allow an integer number of secondary turns or allow integer number of primary layers.

Number of secondary turns (N_S) is calculated by:

$$N_S = \frac{N_P \times 1.15 \times (V_{NOM} + V_{DOUT})}{\sqrt{2} \times (V_{IN-NOM})}$$

N_P – Number of primary turns

V_{NOM} – Nominal output voltage

V_{DOUT} – Output rectifier voltage drop

Note: Assumes 15% load regulation

Number of auxiliary turns (N_{AUX}) is given by:

$$N_{AUX} = \frac{N_P \times 9}{\sqrt{2} \times V_{IN-NOM}}$$

An auxiliary voltage of 9 V is selected to maintain V_{DD} supply under worst case operating conditions, while meeting no-load power requirements.

Figure 3 shows the cross section and schematic of a typical, low-leakage RDFC transformer. The primary winding is multi-layer and wound full-width to achieve maximum coupling. In order to reduce EMI, the primary winding must start from the end connected to the primary transistor collector pin.

A multi-filar, full-width auxiliary winding is used to screen the core from primary. The auxiliary winding at the bottom of winding order ensures V_{DD} supply to the RDFC controller during short circuit conditions.

A wound screen or copper foil screen is used to minimize EMI noise coupling. When using a wound screen, a multi-filer full width winding must be used. The copper foil screen must be single turn and insulated at the ends to avoid a shorted turn.

The secondary winding must be full-width to achieve better coupling. Special care has to be taken to minimize the separation between primary and secondary in order to achieve low leakage inductance.

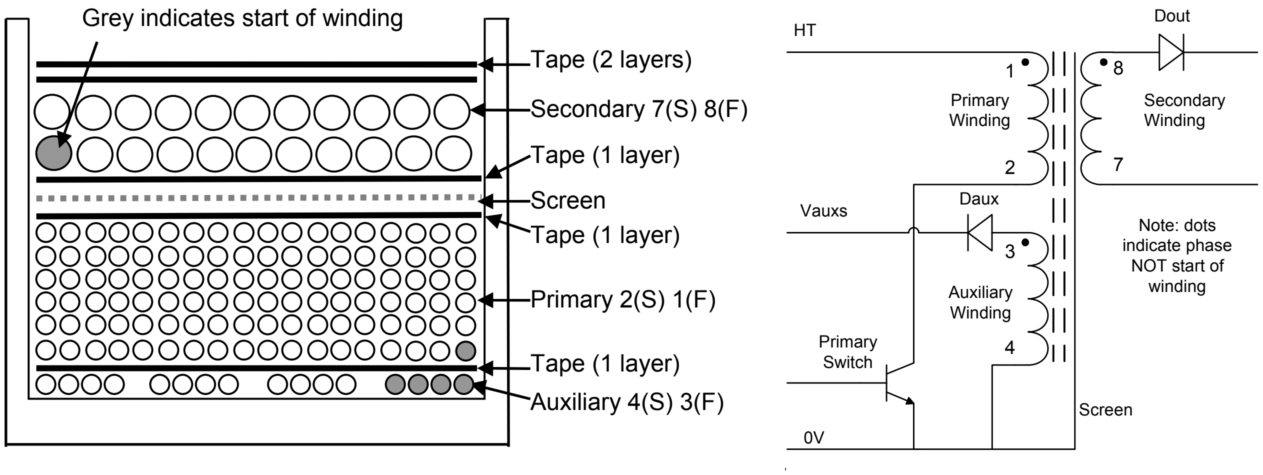

Figure 3: Transformer Cross Section and Schematic
Note: x(S) means start on pin x, y(F) means finish on pin y

Output Capacitor (Cout)

The output capacitor (Cout) attenuates switching frequency ripple at the power supply output. When selecting a suitable Cout, ripple current rating, effective series resistance (ESR), DC voltage rating, size and cost must be considered. Lower RMS output current in RDFC compared to flybacks, due to the on-state current shape, reduces the required ripple current rating of Cout.

Ripple current rating (I_{Cout}) of the Cout is given by:

$$I_{Cout} = 1.155 \times I_{NOM}$$

I_{NOM} – Nominal output current.

Required ESR value of the Cout is given by:

$$ESR = \frac{SwitchRipple \times V_{NOM}}{7/2 \times I_{NOM}}$$

SwitchRipple – Percentage switching frequency ripple at the output

The recommended minimum DC voltage rating (V_{Cout}) for Cout is $V_{Cout} = 1.25 \times V_{NOM}$.

Primary Transistor (Q1)

The primary switch transistor (Q1) is selected with consideration to the following:

- Maximum peak collector voltage (V_{CE}) under worst case operating conditions;
- Peak collector current (I_C) at the over current protection (OCP) threshold;
- Minimum h_{FE} required to deliver the peak collector current with maximum base drive of the RDFC controller;
- Worst case voltage and current stress during turn off;

A detailed primary transistor specification is available in application note AN-2276.

For applications over 18 W and above, heat-sinking of the transistor should be considered. A clip-on type rated at 10 °CW^{-1} could be adequate.

Resonant Capacitor (Ccol) and Cp

Resonant capacitor (Ccol) is critical for achieving correct operation. It allows the switching frequency to be set, provides Q1 collector voltage information to the controller and allows Q1 on-state collector voltage to be programmed.

Ccol's dielectric must be Class 1 material, such as C0G. Other materials may not be stable enough with temperature and age, and may exhibit significant dielectric absorption, which adversely affect the controller's monitoring of Q1 collector voltage. Ccol must be able to withstand high collector voltages. Recommended voltage ratings are 1 kVdc for 115 Vac applications and 1.5 kVdc for 230 Vac applications. Suitable Ccol values are available in the Basic Design Guide, [3].

Capacitor Cp allows Q1 on-state collector voltage to be optimised depending on transistor type and input voltage. For 115 Vac applications using 700 V Vcbo rated transistors, on-state threshold voltage should be set between 2 V to 3 V typically. For 230 Vac applications using 1200-1500 V, Vcbo rated transistors on-state threshold voltage should be set between 4 V to 6 V typically. However optimum on-state threshold voltage can vary depending on transistor type and power supply rating. The Cp capacitor does not need to be a Class 1 type and can be a low voltage type. Suitable Cp values are available in the Basic Design Guide, [3].

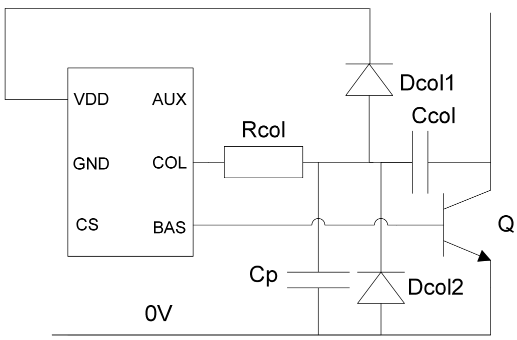

Figure 4: COL Pin Protection Circuit

COL Pin Protection

Diodes Dcol1, Dcol2 and resistor Rcol, shown in Figure 4, protect the controller COL pin from excessive voltage and current. 1N4148 or any other fast recovery diode with at least 0.2 A forward current capability is suitable for Dcol1 and Dcol2. The value of Rcol should be a 220 Ω.

Output Diode (Dout)

The output diode (Dout) must withstand continuous forward current under overload conditions and reverse voltage at peak input voltage. Schottky diodes are recommended due to low forward voltage and short recovery times. However high output voltage applications may require fast epitaxial diodes if Schottky diodes are not available with required reverse voltage ratings.

Minimum reverse recovery voltage (V_{RRM}) is:

$$V_{RRM} = 1.25 \times \left[V_{NOM} + \frac{1.15 \times (V_{RES-PK} - V_{IN-NOM}) \times (V_{NOM} + V_{DOUT})}{\sqrt{2} \times V_{IN-NOM}} \right]$$

V_{RES-PK} = 537 V for V_{IN-NOM} = 115 Vac

V_{RES-PK} = 1078 V for V_{IN-NOM} = 230 Vac

The factor 1.25 provides safety margin and the factor 1.15 allows for load regulation.

Minimum forward current (I_{F-AVG}) rating is:

$$I_{F-AVG} = 1.25 \times I_{NOM}$$

The factor 1.25 provides safety margin. A heat sink may be required on Dout for high output current applications.

Current Sense Resistors (Rcs, R2)

The RDFC controller has two internal threshold values called OCPH (Over Current Protection High) and OCPL (Over Current Protection Low) which are set by the current sense resistors, R2 and Rcs (Figure 5). The OCPH threshold is set so the converter produces rated power under Normal mode and enters Foldback mode when the load is increased beyond a given threshold. OCPL threshold determines the point at which the converter changes from Standby mode to Normal mode and vice versa. Optimal setting of the OCPL threshold gives very low power consumption and eliminates audio noise at low loads.

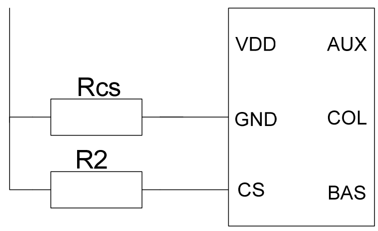

Figure 5: OCPH and OCPL Programming Circuit

The emitter current (I_{OCPH}) that causes the CS pin voltage to equal the OCPH threshold is given by:

$$I_{OCPH} = \frac{5 \times P_{NOM}}{\sqrt{2} \times V_{IN-NOM} \times \eta}$$

The factor 5 accounts approximately for the peak to average emitter current ratio over a mains cycle, controller duty cycle and emitter current shape in RDFC.

R_{CS} is given by:

$$R_{CS} = \frac{0.25}{I_{OCPH} - I_{OCPL}}$$

Where I_{OCPL} is the emitter current that causes the voltage at the CS pin to be equal to the OCPL threshold. Usually I_{OCPL} is selected as a percentage of I_{OCPH}. Typically, I_{OCPL} is 20% of the I_{OCPH}, in which case the value of R_2 is given by:

$$R_2 = \frac{5000}{\left(\frac{I_{OCPH}}{I_{OCPL}} - 1\right)}$$

Aux Pin Supply

Base drive current for the primary switch (Q1) is supplied via the AUX pin of the controller. Qaux must be a BC337-40 or similar high gain transistor. For low power, minimum cost applications, Qaux can be eliminated and Raux can be connected directly to V_{DD}.

V_{DD} Feed Resistor

A V_{DD} feed resistor is required that will provide sufficient supply current to the chip (via the VDD pin) at minimum auxiliary winding voltage (about 6 V) but which dissipates low power (to reduce no-load power consumption). For applications in the range 6 W to 40 W, a value of 1 kΩ is recommended.

REFERENCES

[1] C2472, C2473 Datasheet (DS-1423) www.camsemi.com/support/datasheets

[2] C2471 Product Datasheet (DS-1639) www.camsemi.com/support/datasheets

[3] RDFC Basic Design Guide (DG-1694), www.camsemi.com/support/designguides

[4] J. P. Vandelac & P. Ziogas, “A Novel Approach for Minimising High Frequency Transformer Copper Losses”, IEEE PESC Conf. Record, 87CH2459-6, 1987, p.355-367

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