CamSemi

C2474PW1

PDIP-8 Package

Qualification Test Report

REP-1816-01

26-Jul-2007

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Scope C2474PW1 device manufactured at Atmel Colorado Springs
Assembly in the PDIP-8 package in Unisem Ipoh

Approvals TRB Qualified the above and awarded Production release on 26th July 07

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REVISION HISTORY

Issue	Description of Changes	By	Issue Date
01	C2474PW1 PDIP-8 Product Qualification Report	PJ	26-July-2007

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1 Introduction

1.1 Qualification Overview

The following report details the qualification program completed to ensure the C2474PW1 (in PDIP-8 package) is of a suitable quality and reliability standard for production release. This has been done in accordance with CamSemi Product Qualification and Change Procedure – (CS01-003P), which is aligned with JEDEC standard JESD47. This report includes a product overview, product qualification results and RoHS testing results.

- High Temperature Operating Life (HTOL), Temperature Humidity Bias (THB), Autoclave, Temp Cycle and Construction Analysis have all been tested using 3 independent silicon fabrication lots.
- Latch up, Electro Static Discharge (ESD), Human Body Model (HBM) and Charge Device Model (CDM) tested on 1 lot.
- Hot carrier, Electromigration and Gate Oxide Integrity data has been collected direct from the specific fab / process.
- HTOL performed on SOT23. All other tests completed on PDIP-8.

1.2 General Overview

1.2.1 Product Name

Forward converter controller for offline applications, type number C2474PW1.

1.2.2 Product Application Description:

The C2474PW1 controller is used in applications that typically operate from single rail input voltages. Applications that currently use single rail input Power Supplies are cordless phones, routers and hubs, power tools, audio systems, white goods and so on.

The controller functions in a single ended, Resonant Discontinuous Forward Converter (RDFC) topology, over the nominal power range of 3 W to 40 W.

This type of converter operates off a single rail input voltage and there is no classical feedback for regulation. It offers advantages over linear power supplies as it passes efficiency and standby legislation / codes of conduct where linear power supplies may not. It is also smaller, lighter, has protection features and has output characteristics that can be tailored to the particular application.

1.2.3 Process Technology

C2474PW1 is implemented in a 0.35 µm CMOS tri-layer metal process, which is a 3.3 V nominal process designed for high speed applications.

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2 Process and Package Information:

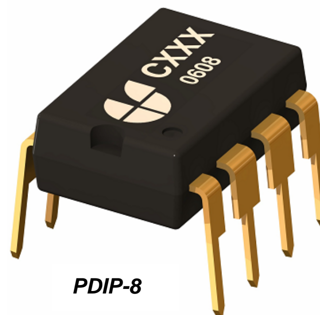
2.1 Wafer Process Summary

Supplier	Process Name	Metal layers	Passivation type	Gate Oxide Material	Metal material	Wafer diameter
Atmel	AT56K CMOS 0.35 µm	3	TEOS + Oxynitride	Silicon Dioxide	AlCu	150 mm

Process options used:

- Double poly capacitor (DPC);
- High sheet resistance poly resistors (HRes)

2.2 Package Summary



PDIP-8

Material/Package		PDIP-8
Supplier		**Unisem - Ipoh**
Lead frame		Copper 194SH with Spot Ag plating
Die attach material		Ablebond 84-1LMISR4
Bond wire:	**Material...**	Gold Thermosonic
	Diameter…	25 µm
Lead plating		Pure matt tin
Mould compound		Samsung SG8300HX
Moisture Sensitivity Level (JEDEC MSL Classification)		Not classified (through hole)
RoHS status		RoHS compliant Report 'REP-1825-01_PDIP-8_RoHS_report' available on request
Flammability rating		UL94-V0

3 Product Qualification Results

3.1 Results Table

Test Name See Section 10 for test details	Pass Requirement (parts tested/allowed failures)	Results			Overall Pass/Fail
		Sub Lot 1 (FAA3)	Sub Lot 2 (FAA7)	Sub Lot 3 (FAA6)	
HTOL **(Performed on SOT23)**	77/0 for 1000 hr	154/0	80/0	80/0	Qualified by similarity to SOT23
THB	77/0 for 1000 hr	80/0	80/0	80/0	**Pass**
Autoclave	77/0 for 96 hr	80/0	90/0	90/0	**Pass**
Temp. Cycle	77/0 for 500 cycles	100/0	90/0	90/0	**Pass**
Construction Analysis	No faults after temp cycling (look for die crack / Pattern shift / Package delamination)	Completed – no faults found	Completed – no faults found	Completed – no faults found	**Pass**

3.2 Electro Static Discharge / Latch Up Results

Completed on 1 lot for each package type:

	Latch up		ESD – HBM (amount tested / failures)	ESD – CDM (amount tested / failures)	Overall Pass / Fail
	I test	V Supply			
Pass requirement	6/0 @ ± 100 mA	6/0 @ 1.5 x Vdd	3/0 @ 2000 V	3/0 @ 500 V	
Requirement	**Curve trace and ATE test (ref JEDEC)**				
Data	6/0	6/0	6/0 @ 3000 V	6/0 @ 600 V	**Pass**

3.3 FIT rates

High Temp Operating Life (HTOL) tests on Silicon foundry test devices shows typically 1M power-on hours per year with Zero early life failures and Zero 1,000 hr failures giving 0ppm EFR and ~20 FIT.

CamSemi has also calculated (using the Arrhenius model) FIT rates based on the HTOL data gathered from the C2472PX2 qualification. The total device power on hours during qualification has been calculated to 315920 hr, and using a 60% confidence level and 0.7 eV activation energy the FIT rate is ***19 FIT***, with a Mean Time Between Failures (MTBF) of ***6168 years***, based on 55 °C average use junction temperature.

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4 Wafer Level Reliability

The following wafer level data has been referenced from the Atmel WLR and Qualpak AT56K reports.

4.1 Hot Carrier Qualification

Gate Oxide has been subjected to stress to determine lifetime due to Hot Carrier Injection. The 3.3 V oxide was subjected to a Vd = 3.6 V for 10% IDSAT shift for a 10 / 0.35 µm NMOS transistor. The DC results were 0.27 years which is equivalent to > 10 years for AC operation.

4.2 Electromigration

Electromigration testing was performed on six structures, which included Contact, Metal 1, Via 1, Metal 2, Via 2, and Metal 3. The conditions of the tests were 2 x 10^6 Acm^{-2} current density at an ambient temperature of 200 °C. The testing was terminated at 1017 hours. With the exception of Metal 2, there were no failures. In order to estimate a minimum life expectancy for the zero failure tests, time to first failure is calculated as if occurring at 1017 hours of stress time.

The calculated life time for the metal stack failure (based on 0.1% population failure) was 77 years for metal 2. Life time for contact, Metal 1, 3 and both Via stacks exceeded 650 years. This exceeds the requirement of 10 years.

4.3 Time Dependent Dielectric Breakdown

Three wafers were selected from lot 9G3470 for constant field accelerated stress. Gate oxide thickness varied from 72.9 Å to 74.7 Å with a target of 70 Å. For all stresses, voltages were chosen so that oxide fields were consistent wafer to wafer.

The capacitors used for this study were GATE2_FIELD_EDGE in WLR_C. Each has 6,267 square microns area. Forty-six sites were stressed at temperatures between 175 °C and 225 °C at 9.5, 10.0, and 10.5 $MVcm^{-1}$. Using the ‘E’ model and extrapolating to use conditions of 105 °C at 3 V +10% and 63 Å gate oxide thickness (10% below target), the estimated time to reach 0.01% failures is about 635 years, which exceeds the design requirement of 10 years.

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5 Qualification Test Methods Reference

Test	Conditions	Reference	Pass requirements
HTOL	125 °C, 1000 hr, VDD = 4 V	JESD22-A108	Electrical functional
THB	85 °C, 85 % RH, 1000 hr VDD = 4 V	JESD22-A101	Electrical functional
Autoclave	121 °C, 2 atm 96 hrs	JESD22-A102	Electrical functional
Temp. Cycle	Condition C, -65 °C to +150 °C, 15 min dwell, 500 cycles	JESD22-A104	Electrical functional
Construction Analysis	Parts to have been subjected to temperature cycling test.		No pattern shift
Latch Up		JESD 78	I test requirement ± 100 mA supply over voltage(1.5 x Vcc) ATE Functional tests at 25 °C
ESD - HBM	2 kV	JESD22-A114B	Electrical functional
ESD - CDM	500 V	ESD SDM5.3.1-1999	Electrical functional
Hot Carrier		JESD28-A	>10 year lifetime
Electro migration		JESD61	>10 year lifetime
Gate Oxide Integrity		JESD35A	>10 year lifetime

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