

INTRODUCTION

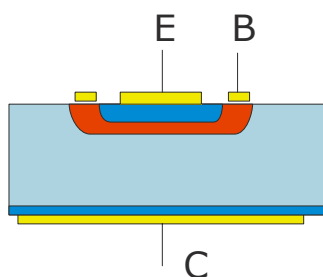
This application note relates to the resonant discontinuous forward converter (RDFC) offline power conversion topology and CamSemi's C2470 series RDFC controller ICs [1].

The C2470 controllers are designed to work with a low cost bipolar junction transistor (BJT) as the primary power switch. It is important to understand certain key characteristics and behaviours of the high voltage BJT to ensure that a suitable type is selected and your RDFC application design is well centred. This application note addresses some important BJT characteristics, and how types of transistors can be assessed for use in an RDFC application. The key characteristics are:

- Breakdown voltage (e.g. V_{ce0} , V_{cbo} , V_{ces})
- Turn off behaviour and RBSOA
- Gain (h_{FE})

HIGH VOLTAGE BIPOLAR TRANSISTOR BASICS

High voltage BJTs have essentially the same construction as low voltage ones. Taking an NPN transistor as an example, an n-type wafer is first doped with the p-type base region and then an n-type emitter region. The wafer backside is the collector connection and metallisation is applied to connect to the base and emitter regions as shown below.

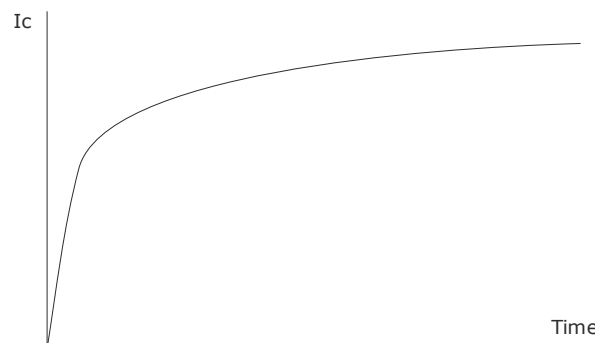


The bulk of the material is lightly doped n-type (N-), the base and emitter regions are more heavily doped. Commonly a fourth region is doped into the wafer, a heavily doped n-type layer at the backside of the wafer to assist with making a good connection for the collector. This construction is known as "triple diffused". The principal difference between low and high voltage bipolar transistors is the thickness of the N- region. In high voltage transistors, this region must be very thick to withstand high voltages when turned off. The layer thickness has a very strong influence on the turn on and turn off behaviour the transistor.

When the transistor is off and a high collector voltage is applied, the electric field between base and collector causes depletion of this N- region and turns it into an insulator. The voltage withstand of the transistor in this condition is dependent on the insulation properties of the depleted region. When the transistor is turned on two things have to be achieved a) emitter current has to be established (conventional transistor action) and b) the N- region has to be turned into a conductor. (a) happens very quickly but (b) takes place in two stages:

1. Depletion region retreats (quick)
2. Charge diffuses into the N- minus region causing a reduction in resistivity (slow)

The consequence is a two-step turn-on process. When (excess) base current is first applied, depending on the load characteristics, the collector current rises quickly to an initial value and then continues to rise - but much more slowly. This can be observed if the transistor is operated at a constant low collector voltage of, say 10 V:



Initial rise of collector current operates in a timescale of tens of nanoseconds, the subsequent rise takes place over microseconds or tens of microseconds, and varies between manufacturers even for the same nominal transistor type. A simple model is a perfect transistor with a resistor in series with the collector. When excess base current is applied the transistor turns on very quickly (to a low "internal" collector voltage) but the collector voltage is determined by the series resistor and the current flow. The value of the resistor subsequently falls as charge diffuses into the collector region. The on-state condition of the transistor is often characterised as:

Quasi-saturation: low diffusion of charge into the collector region so resistance causes a collector voltage of several volts at moderate currents.

Hard saturation: high levels of charge in the collector region to minimise resistivity, so the collector saturation voltage is as low as possible.

The behaviour of the transistor at turn off is complex and depends on

- Transistor type
- Previous on-state conditions
- Base control

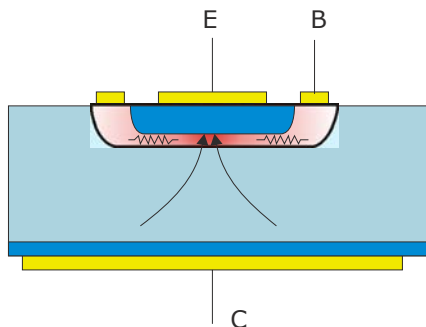
To stop collector current flow, it is necessary to:

- Stop "transistor" action by reducing the internal base-emitter voltage, so the base-emitter junction is no longer forward biased
- Remove remaining stored charge, particularly in the collector region

A good discussion of the physics and processes involved is given in [2]. Two key factors have to be taken into account:

If during the on-state, a high excess base current was applied and the collector voltage was low, there will be large amount of excess charge in the transistor. Much of this charge has to be removed through the base connection and a significant negative base current is needed if this is to be done quickly.

If high negative base current is applied very quickly then a condition can arise where part of the base region becomes depleted of charge and becomes a high resistance, "isolating" residual charge under the emitter and this takes a long time to remove:



When this condition occurs there can be a long tail to the current at turn off. Further, this remaining current flows in a concentrated region in the centre of the emitter, causing higher levels of local heating and potential for device damage.

There is a simple trade-off between the level of saturation in the on-state and the turn off speed of the transistor. For fast turn off it is necessary to operate in the on-state with minimum excess base current and avoiding low collector voltage. There has to be a compromise because high collector voltage during the on-state can cause low efficiency and high power dissipation in the switching device.

The proportional base drive (PBD) system in the RDFC controller permits setting the on-state voltage to suit the type of transistor. Generally, transistors with higher voltage rating will need to be operated at higher on-state collector voltage. Also, for higher on-state current (in relation to the transistor current rating), higher on-state voltage should be allowed. The choice of on-state collector voltage depends on the transistor type, maximum collector current and allowable power dissipation. In extreme cases, the on-state collector voltage may need to be as high as 10 or 15 V if excessive turn off time and stress is to be avoided.

If under any conduction conditions a high collector voltage is applied then the depletion region will extend into the N- collector region. Virtually all of the externally applied collector voltage appears as a potential difference across the depletion region. Charge carriers in the region are accelerated by the electric field and gain energy. If the electric field is strong enough, the carriers gain sufficient energy to ionise atoms in the crystal before leaving the region, and this ionisation causes additional collector current flow. At higher levels of collector voltage (causing higher electric field), the additional charge carriers generated by the collisions are accelerated by the field sufficiently to cause further ionisation and current flow. Eventually the current flow increases exponentially. This is avalanche breakdown. However, it need not be destructive; it all depends on how much local heating occurs. If the collector voltage is maintained at a high level while the high current flows then very high power levels are developed in the collector region, causing local heating and device damage. If however, the collector voltage falls then the power will be reduced and device damage might be avoided.

BREAKDOWN VOLTAGES

Consider a transistor with no established current flow. Apply a high voltage between base and collector with collector as positive and with the emitter connection open. A depletion region is established in the N- collector region and the applied voltage largely appears across the depletion region. A low level of charge carriers is generated in the depletion region by thermal activity and are accelerated by the electric field. With sufficient applied field, the charge carriers cause ionisation of atoms in the crystal leading to additional current as described above. As the applied voltage is increased eventually leading to an exponential increase in collector current. This is the condition specified in datasheets BVcbo i.e. collector-base breakdown with emitter open.

If however, the voltage is applied between emitter and collector with the base open then the behaviour is more complex. Ionisation in the collector region causes charge carriers, electrons migrate to the collector and holes towards the base. With the base connection open there is an opportunity for current amplification by transistor action of the current arriving in the base region. The amplified current becomes collector current, which adds to the charge carriers moving in the collector region. With sufficient electric field the charge carriers can cause further ionisation. The net result is that breakdown in this configuration (BV_{ceo}) occurs at a lower voltage than if the voltage is applied between base and collector with the emitter open. Suppose however that the voltage is applied to emitter and collector but the base terminal is shorted to the emitter terminal. In this case the current arriving in the base region will exit by the base connection so cannot be amplified by transistor action. Breakdown voltage in this configuration is referred to as BV_{cesm} , and is normally very similar to the value of BV_{cbo} . Instead, if the base is connected to the emitter by a resistor and voltage is still applied between emitter and collector then the relevant rating is BV_{cer} . It is essential that the resistance value is specified. For resistances below about 1 k Ω , BV_{cer} is indistinguishable from BV_{cesm}/BV_{cbo} . With high resistance values there is the opportunity for the collector leakage current to develop sufficient voltage across the base emitter junction to cause current gain by transistor action, and the breakdown voltage is reduced.

The RDFC controller turns the bipolar transistor off by shunting the base to the emitter by a low resistance on-chip transistor. The maximum resistance of this transistor is specified in the datasheet and is sufficiently low to ensure that the relevant rating for transistor in the off-state is BV_{cesm} .

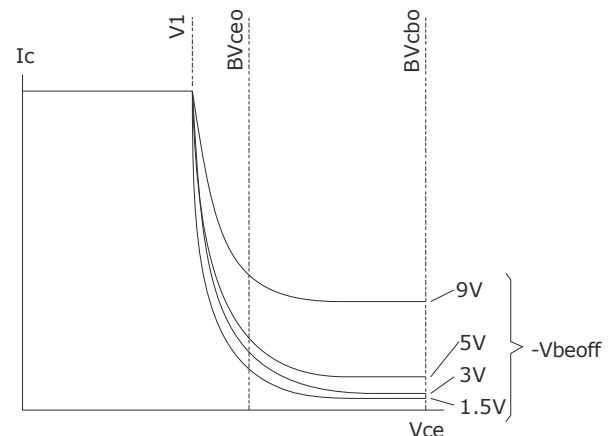
RBSOA

This is the "reverse bias safe operating area" and refers to the safe turn off of bipolar transistors. "Reverse bias" refers to negative voltage applied to the base terminal relative to the emitter. The RDFC controller does not apply negative based bias for turn off, instead it connects the base emitter by a low resistance path, but similar principles apply.

There are complex processes involved in turn off of bipolar transistors, and particularly for high voltage types where significant charge has been stored in the collector region. See [2] for a detailed discussion. To stop the flow of collector current it

is necessary to remove the charge from the base and collector regions and to remove the forward bias of the base emitter junction. This requires current flow out of the base terminal. As explained above, the lateral resistance of the base region is important, and this varies according to how quickly base charge is removed. During the turn off process, current concentrates into the centre of the emitter and this can lead to secondary breakdown in the adjacent collector region.

Transistor manufacturers sometimes publish RBSOA curves as guidance for appropriate turn off design. However the data is often not comprehensive and does not cover the condition $V_{be} = 0$ V so a degree of interpretation is required. The RBSOA depends on a number of parameters including conditions in the on-state and the turn off drive to the base. A typical set of curves would look like:



As well as looking at the RBSOA curves for a particular transistor, it is important to look at the test conditions that are specified. Typically the on-state conditions apply a very high level of excess base current, with consequent low on-stage collector voltage. This means that the collector region has a very large amount of excess charge before turn off. In an RDFC-based application, collector voltage is managed by the proportional base drive system to minimise the excess collector charge and to operate the transistor in quasi-saturation, rather than hard saturation (low collector voltage).

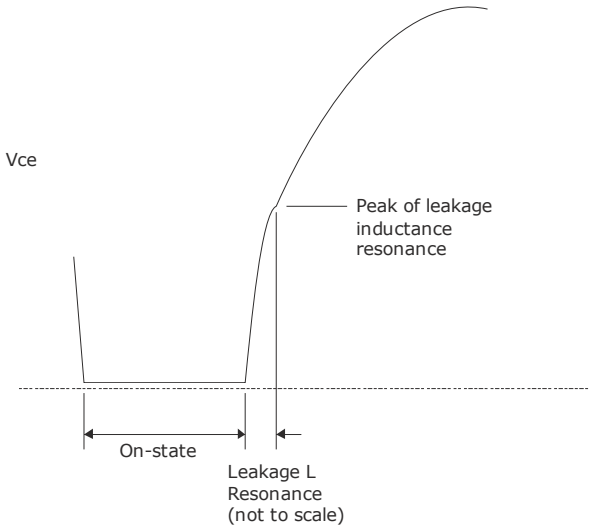
Other differences between the BJT test configuration and RDFC applications are:

- Lower rate of collector voltage rise because of total collector node capacitance (C_{ctot})
- Current available from the inductor (transformer leakage inductance) will fall more quickly because of lower inductance

Note: The total collector node capacitance (C_{ctot}) is the sum of:

- Transformer primary capacitance (C_{pri})
- COL pin capacitor (C_{col})
- Collector capacitance of the BJT (C_{bc}). Refer to "Transistor collector output capacitance C_{ob} " on page 10
- Any other capacitor connected between the collector and emitter for application purposes (C_{colgnd})

In RDFC applications at transistor turn off there is a fast rise of collector voltage caused by energy stored in the transformer leakage inductance. Suppose the BJT switches off instantly then the collector voltage will rise as a resonant waveform of the leakage inductance (L_{leak}) and C_{tot} . At the top of the resonance, no current is available.



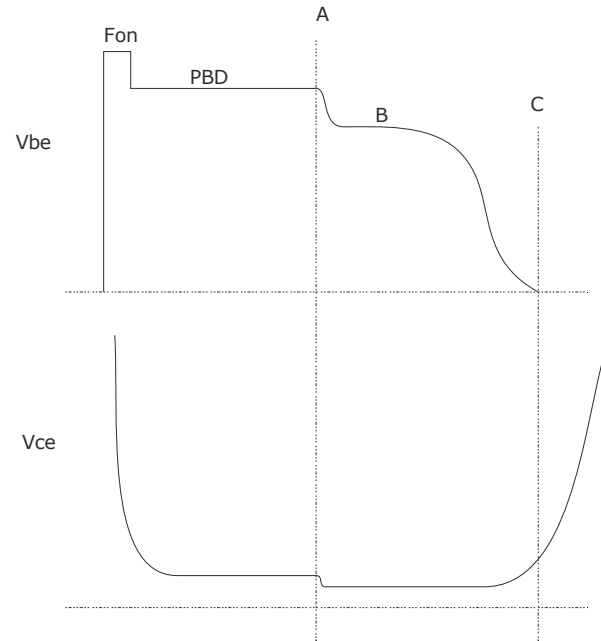
The BJT does not turn off instantly, so it continues to pass current as the collector voltage rises. There will be a "trajectory" of V_{ce} and I_c during the leakage inductance resonance, and it is necessary to judge whether this is likely to be damaging. Referring to the graph above, if I_c has fallen to about zero by the time $V_{ce} = V_1$, there will not be a problem at any V_{be} .

Judging the point where $I_c = 0$ is best done using a current probe in the collector connection; not the emitter because there is significant negative I_b , which reduces I_e in relation to I_c . However it is likely that $I_c = 0$ occurs before the leakage inductance resonance peak.

Another useful measurement is the base and collector voltage waveforms as shown below.

The controller tries to turn the BJT off at A, but there is stored charge that keeps it conducting. Plateau B represents negative current coming out of the BJT, developing voltage across the on-chip base-emitter clamp transistor. Eventually the charge is mostly removed and the BJT will no

longer support the I_c , so the collector voltage rises. Because most of the collector current is coming out of the base, point C indicates approximately when collector current has stopped.



If there is collector current still flowing when there is significant V_{ce} , it is necessary to look at the V/I trajectory and decide if it is likely to be a problem. Suppose some I_c was seen at $V_{ce} = V_1$, but it had stopped by the time $V_{ce} = V_{ce0}$ then it may be judged as acceptable.

Once the transistor has been off for some time, $V_{ces} (\approx V_{cbo})$ applies, so the resonance peak can go higher because it is long after the charge has been removed.

An approximate rule that indicates whether there could be an issue is check whether the peak voltage of the leakage inductance resonance $> V_{ce0}$. If so, further investigation of the V/I trajectory is needed. If there is a problem:

- Decrease the OCPH threshold current (refer to the Power Control section in the RDFC controller datasheet [1] for further information)
- Decrease transformer leakage inductance (L_{leak})
- Increase C_{tot} by adding capacitance between BJT collector and emitter (but check for core saturation)

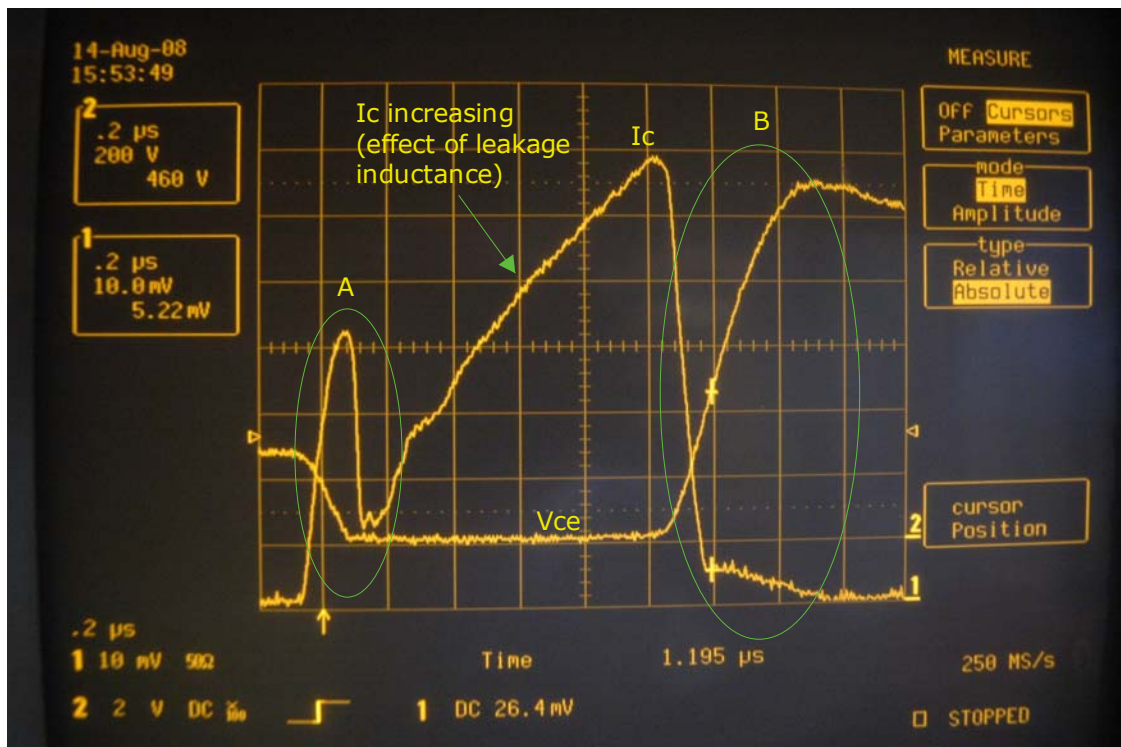
Note also that worst conditions typically occur in short circuit at high mains/surge, because the BJT storage time causes increased I_c and the leakage inductance acts from nearly HT, rather than HT - reflected output voltage. The traces below were taken from a 220 Vac application operating into an output short-circuit and with the BJT heated.

Because the output voltage is low, the on-time is very short and current is rising very quickly in the collector (limited by the leakage inductance of the transformer). Two particular features of this trace are worth noting:

A: At turn on, the collector voltage falls rapidly from a high voltage because the resonance has not brought the collector down to a low voltage. A pulse of collector current flows due to circuit capacitance charging (e.g. C_{col} and C_p of the transformer).

H_{FE} AND BASE DRIVE CURRENT

For proper converter operation, it is necessary that the RDFC controller can provide sufficient base current drive to the primary switch transistor to ensure the transistor is turned on under all operating conditions. If there is insufficient base drive then the collector voltage will rise and the COVP protection function will operate, putting the controller into burst/foldback mode.



B: At turn off, the collector voltage rising quickly causes current flow through the base-collector capacitance.

In the conditions at B, the collector current should be related to the rate of collector voltage rise via the transistor base-collector capacitance. In the example above the collector rises by about 500 V in approximately 150 ns, producing a collector current of about 50 mA (the scale is 100 mA per division). This corresponds to a capacitance of about 15 pF, consistent with expected output transistor capacitance used. For consideration of RBSOA, we can assume that transistor conduction has ceased by approximately the start of the "shelf" shown in B (i.e. where the oscilloscope trace cursor is positioned). In this example, the collector voltage is about 460 V at the point where the collector current has fallen to a low value.

Applications should be designed so that:

Maximum required collector current in all modes < OCPH threshold < Collector current available from BJT

If the OCPH threshold is less than the collector current available from the BJT, then there is a risk that the controller will hold the transistor in conduction without terminating the on-time early; passing a large current but without being held at a low collector-emitter voltage. There will be high power dissipation in the transistor causing heating and possible failure.

The OCPH threshold should be set to the minimum value needed to provide the required output current under rated-load and start-up conditions.

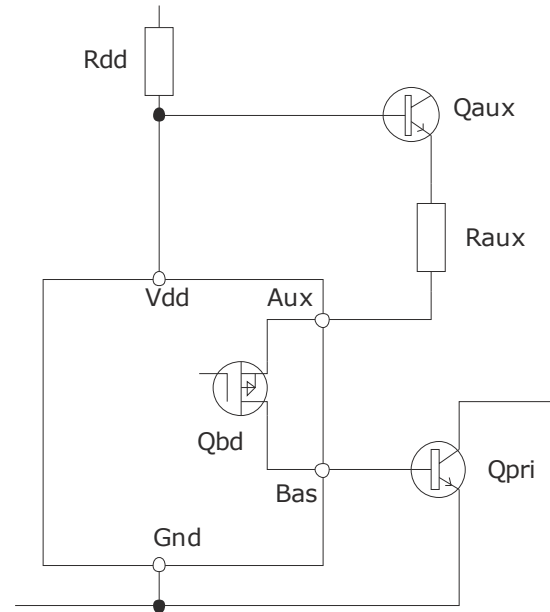
Collector current available from the transistor depends on the transistor type, the on-state collector voltage (preset by the PBD) and base current available from the controller.

The current gain between collector and base current for the transistor is described in the h_{FE} curves and the minimum h_{FE} specifications in the transistor datasheet. Transistor gain reduces at:

- Low device temperature
- High device temperature
- Low collector current
- High collector current
- Low collector voltage

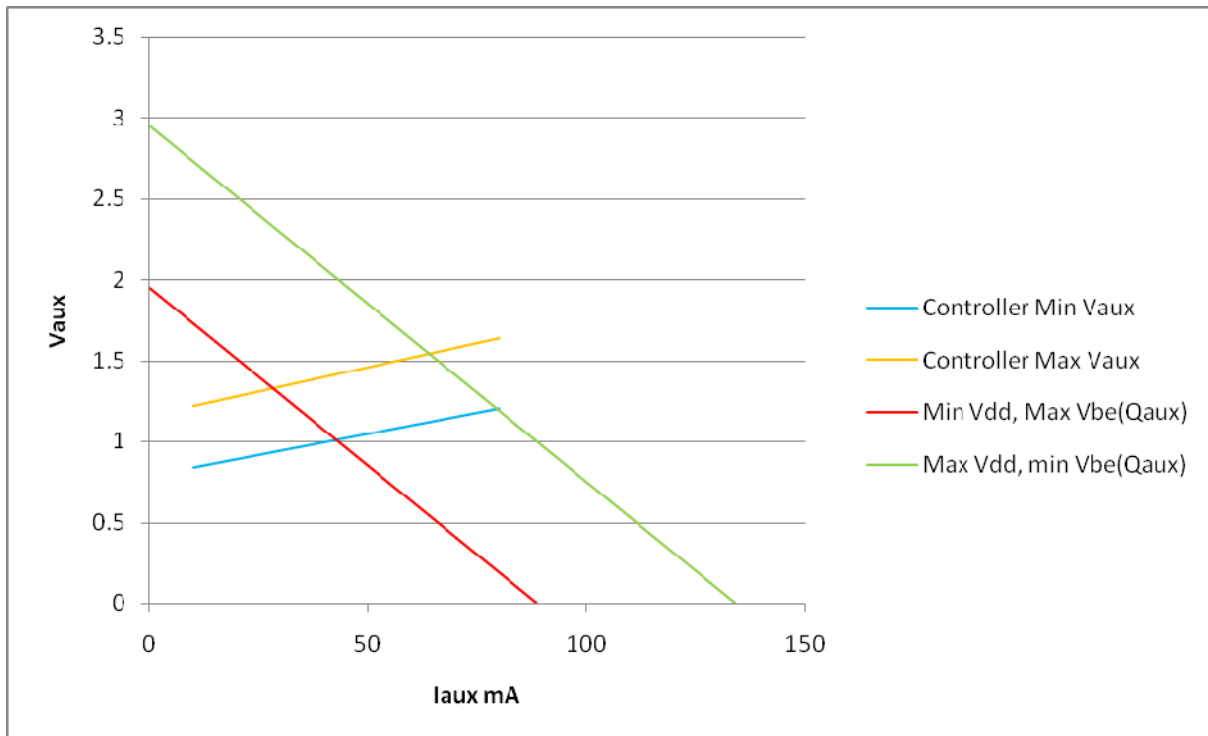
Normally minimum h_{FE} specifications in the datasheet do not match the relevant operating points in the converter application. Secondly, the h_{FE} curves in the datasheet normally are typical values rather than minimum. Hence, a degree of interpretation is required to estimate minimum h_{FE} at the critical operating points. This can be done approximately by factoring the h_{FE} curves according to one or more of the minimum h_{FE} specifications and allowing for some degradation at temperature extremes. Note that the relevant temperature is the temperature of the die within the transistor package, which can be considerably higher than the ambient temperature in the converter.

The RDFC controller datasheet gives the minimum guaranteed base drive capability. However, it is necessary to take account of voltage drops due to the primary switch transistor base-emitter voltage, the auxiliary resistor and auxiliary transistor.



The base of Qaux is held at Vdd, which may be as low as the V_{UVDTHR} . This voltage must support the sum of the following:

- V_{be} for Qaux
- $I_{bas} \times R_{aux}$
- Voltage drop of Qbd
- V_{be} of Qpri



The controller datasheet has several relevant parameters:

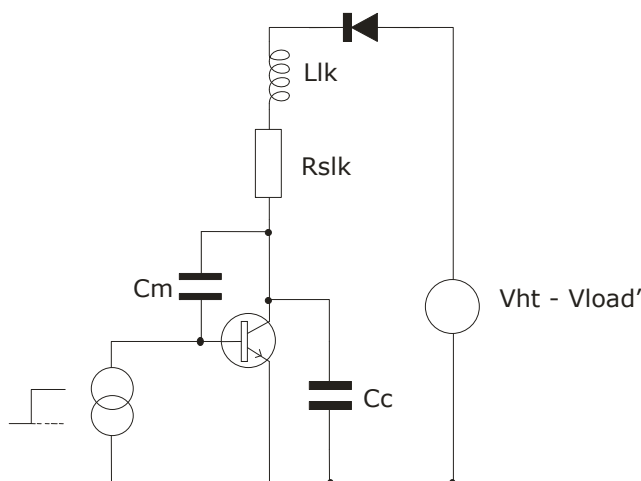
- V_{UVDTHR}
- V_{AUXFON}
- I_{BASMAX}

The maximum available base current depends on R_{aux} , so it is necessary to construct a load line graph to take into account the Q_{bd} characteristic and R_{aux} (see previous diagram). The zone bounded by the four lines represents the possible range of I_{aux} (max).

FBSOA

When transistors are operated with positive base current and collector current, they must be kept within the “forward bias safe operating area”. This takes into account such effects as thermal limitations on bond wires, secondary breakdown and avalanche. See [2] for further discussion. The short on-time of RDFC based converters (typically less than 20 μs) normally means that transistors can withstand relatively high currents or voltages, or combinations of the two. At turn on and during the converter on-time, the collector voltage is normally less than or equal to the HT voltage and collector current is limited by the action of the OCPH threshold. Worst-case conditions typically apply when the converter is operated from maximum mains input voltage and with a short-circuited output. In these conditions, the transistor operates with a very short on-time and high current. The collector voltage during this time may not be very low (due to slow turn on). However, even in these conditions it is unlikely there will be problem in relation to FBSOA.

TURN-ON BEHAVIOUR

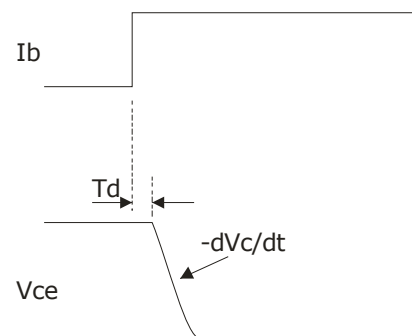


During turn on, the circuit conditions experienced by the BJT are shown in the simplified circuit above. A pulse of constant base current is applied to turn the BJT on. The collector voltage will have been at some positive voltage, dependent on the RDFC operating mode etc. As the collector voltage falls, the total capacitance of the collector node (C_c in the diagram) is discharged. Note that this is made up of several components including the application C_{ool} , parasitic capacitance of the transformer primary, external capacitance connected between collector and emitter, and capacitance in the transistor. In addition, there will be some Miller capacitance, C_m . Apart from winding capacitance, the transformer presents a resistive/inductive load to a voltage that depends on PSU output voltage. When the PSU is loaded lightly the output voltage, referred to the primary, will approximately match the HT voltage, so $V_{ht} - V_{load}$ will be low. At high loads, the PSU output voltage will fall so $V_{ht} - V_{load}$ increases. This means that increasing output load causes a faster increase of on-state current, though it is always mostly inductive (starting from a low initial current) due to the leakage inductance L_{lk} .

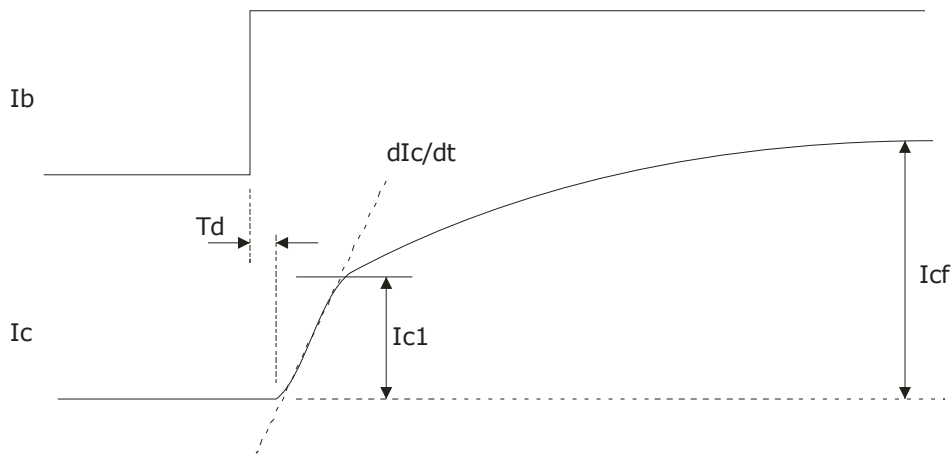
We can consider two regimes of RDFC:

- Low load/Standby B, where the collector voltage falls from a high voltage but there is little collector current through the transformer since $V_{ht} - V_{load}$ is small.
- High load/Normal, where the collector is at a lower voltage before turn on (due to off-state resonance) but the collector current ramps up rapidly since $V_{ht} - V_{load}$ is large.

Low Load/High Initial Vce:



There are two predominant components to the collector voltage fall time: a delay (T_d) where the base region fills with charge, and a second rate-limited fall. The latter is determined by applied I_b acting into C_m , speed (f_T) and gain (h_{FE}) of the transistor, and the remaining collector load capacitance. These are usually more critical in high-line applications where applied I_b is lower (to avoid excessive charge storage, but T_d increases) and the required fall of collector voltage is larger.



In applications where the collector node capacitance (excluding the transistor) is low, the speed will be determined mainly by Miller capacitance, and good performance will require a low capacitance transistor. Generally, the transistor's capacitance increases with current handling capabilities. So, it is important to match transistor "size" to the application: too large can give poor results, just as can too small.

High Load/Low Initial Vce:

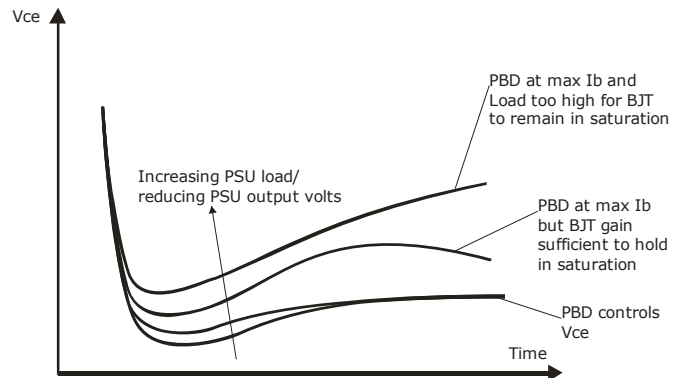
If a low constant Vce is applied to a transistor and then it is turned on with a flat-top base current pulse, the collector current follows a 3-stage pattern.

- Delay Td, while the base region charges
- Fast rise of collector current up to a limit Ic1
- Continuing rise of Ic but at slower time constant, to Icf

Step 1 is similar to the low load/high initial Vce regime. In Step 2 conventional transistor action takes place at a speed limited principally by the transit time (f_T). However this ceases before maximum current is achieved. This is because high voltage transistors normally have deep, lightly doped collector diffusions (necessary to withstand high voltage in the off-state). In the on-state, these regions present a high resistance initially after turn-on. Subsequently, as charge diffuses, resistance falls. When excess charge is present, "hard saturation" is achieved – characterised by low saturation voltage at high current. However the excess charge has to be removed at turn off, delaying the turn off transition. If the base current is limited, the transistor can be held in quasi-saturation where the resistance is reduced, but to an intermediate value, and there is limited excess charge. Turn off is faster but the penalty is higher collector voltage at a given collector current. RDFC is intended to operate in this quasi-saturation mode. The degree of saturation can be

set by choosing the Vce/Vcol attenuation ratio using the Ccol and Cp capacitors.

At high load and short on-time, the quasi-saturation characteristics become important in determining the achievable on-state Vce. Note also that since the load is inductive, the collector current is rising while the ability of the transistor to withstand it also increases due to the quasi-saturation diffusion time constant. Typically, collector voltage traces like this may be observed:



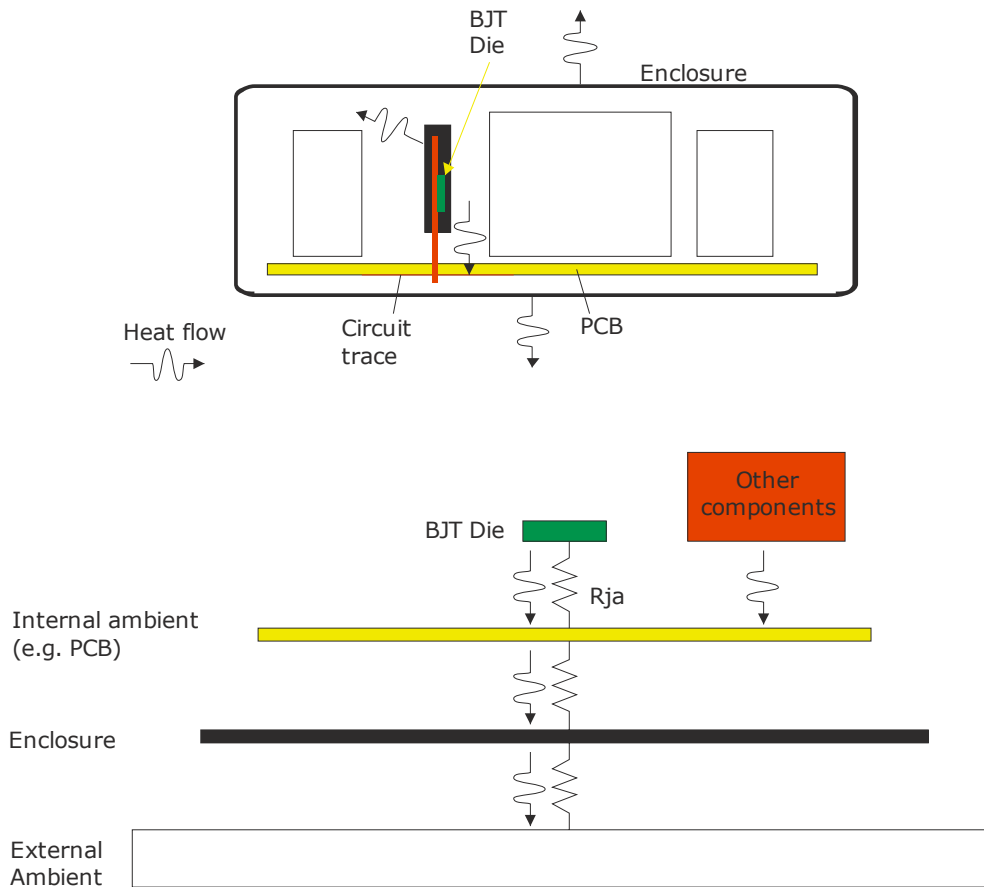
Apart from h_{FE} , important BJT characteristics are:

Transit time (f_T): determines rate of rise of Ic in Step 2

Collector diffusion resistance: determines achievable Ic1 (depending on Vce)

Diffusion time constant: determines how quickly transistor can support higher current in quasi-saturation

Unfortunately, these parameters are rarely described in datasheets and differ significantly between devices. It is recommended candidate transistor types be evaluated under operating conditions relevant to the target applications. It is helpful to test sample transistors in simple test circuits to judge basic device capabilities, as well as in the target application.



THERMAL LIMITATIONS

Power dissipation in the primary switch transistor will cause heating of the die within the package and heating of the package as a whole. Dissipation of power in other converter components will also add to temperature rise inside the enclosure.

For the transistor, the important parameter is the die (junction) temperature under different operating conditions. Power in the transistor transfers to the local “ambient”, such as the PCB or air within the enclosure. The local ambient temperature rises above the ambient temperature external to the enclosure because of power flow through the thermal resistances between the components and the enclosure, and between the enclosure and the external ambient. When judging transistor temperature rise it is important to specify the test conditions, not only for electrical parameters but also for ambient temperature and heat loss conditions external to the enclosure. Typically these might be specified as:

- 45°C still air (not in a fan-assisted oven)
- 25°C ambient, but with converter wrapped in a (specified) blanket

Thermal specifications of transistors normally include:

- R_{ja} = thermal resistance between junction and ambient
- R_{jc} = thermal resistance between junction and case (of the transistor)
- T_{jmax} = maximum junction temperature

R_{jc} is used when the transistor is fixed to a heatsink, in which case the rise of die temperature above the heatsink temperature can be calculated. In many RDC applications there will be no heatsink attached to the transistor and in this case R_{ja} applies. However, these parameters are useful only if the transistor power dissipation is known. It can be very difficult to predict transistor power dissipation, particularly under conditions of short on-time. If transistor power dissipation is moderately low (e.g. < 2 W) then the transistor case temperature is a good guide to the junction temperature because there will be a small temperature difference across the junction-case thermal resistance. A typical test would be to fix a thermocouple to the outside of the transistor plastic body, adjacent to the location of the packaged die. The converter is then operated under some load and ambient conditions and the maximum transistor temperature monitored.

Though the transistor may have a T_{jmax} of, say, 125°C , it is not recommended to operate the transistor at or near this temperature, except in extreme conditions. Reliability of semiconductor devices reduces rapidly when the die temperature exceeds about 115°C . In addition, several important parameters of the transistor degrade with increasing temperature. A particular case is the on-state quasi-saturation parameters and the turn off speed. A common failure mode in overload is when increasing die temperature causes degraded transistor performance that in turn increases the transistor power dissipation, further degrading performance. A given design may operate satisfactorily at an ambient temperature of 25°C with a die temperature of 90°C . However, if the ambient temperature is increased by 20°C , the higher die temperature degrades performance. The transistor dissipation increases further causing die temperature much in excess of $90^{\circ}\text{C} + 20^{\circ}\text{C}$, leading to failure.

TRANSISTOR COLLECTOR OUTPUT CAPACITANCE C_{OB}

This is the capacitance measured across the collector and base terminals with the emitter open. In RDFC converters, this capacitance adds to the total primary capacitance in respect of resonance and rise of collector voltage due to leakage inductance energy. In datasheets it is normally specified at a low voltage (e.g. 10 V), so it is an overestimate of capacitance in normal converter operation because capacitance falls with increasing collector voltage. The applicable capacitance can be estimated either by taking a fraction of the datasheet value (e.g. $\frac{2}{3}$ or $\frac{1}{2}$) or, preferably, by measuring a sample.

REFERENCES

Please obtain the latest version of CamSemi documents from www.camsemi.com.

- [1] C2472, C2473 Datasheet, RDFC Controllers for Offline Applications, CamSemi datasheet (DS-1423)
- [2] Power Semiconductor Applications, Chapter 1, Introduction to Power Semiconductors, Section 1.3 High Voltage Bipolar Transistors, Philips Semiconductors (NXP), <http://www.nxp.com/acrobat/applicationnotes/APPCHP1.pdf>
- [3] Measuring Primary Switch Collector Voltage In RDFC Applications, CamSemi application note (AN-2497)

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